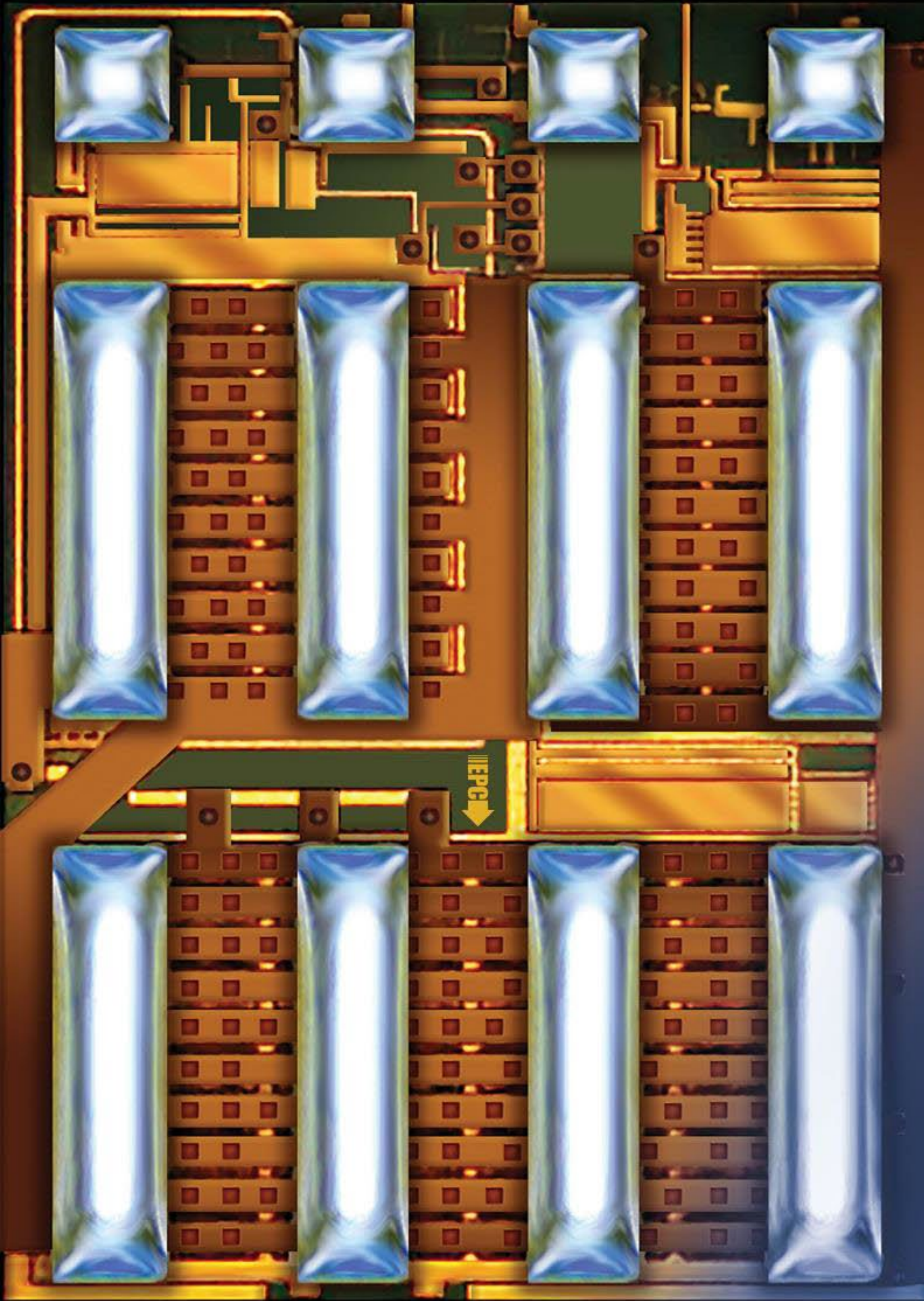


Design Tips to Maximize the Performance of GaN-Based Designs

Brian Miller

EPC
EFFICIENT POWER CONVERSION

Agenda

- GaN Technology Review
- Driving GaN FETs
- Layout techniques and the importance of inductance
- Overview of the PCB based thermal system
- Adding a heatsink to GaN Devices

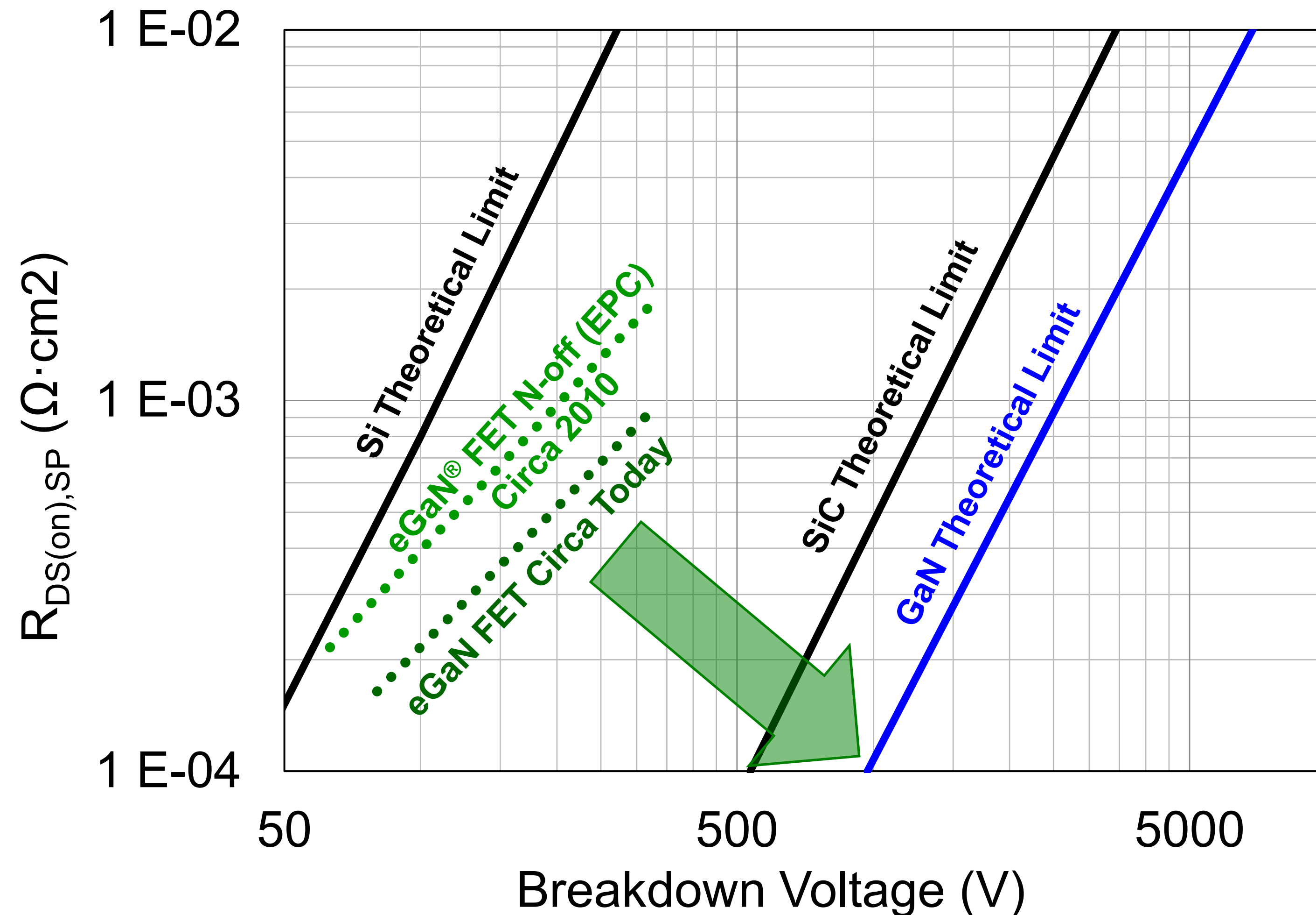
GaN FET Characteristics

- GaN FET key metrics
  - Reverse Recovery
  - Reverse Conduction
  - Switching Characteristics
  - Miller Ratio
  - Reliability

Key GaN FET Performance Metrics

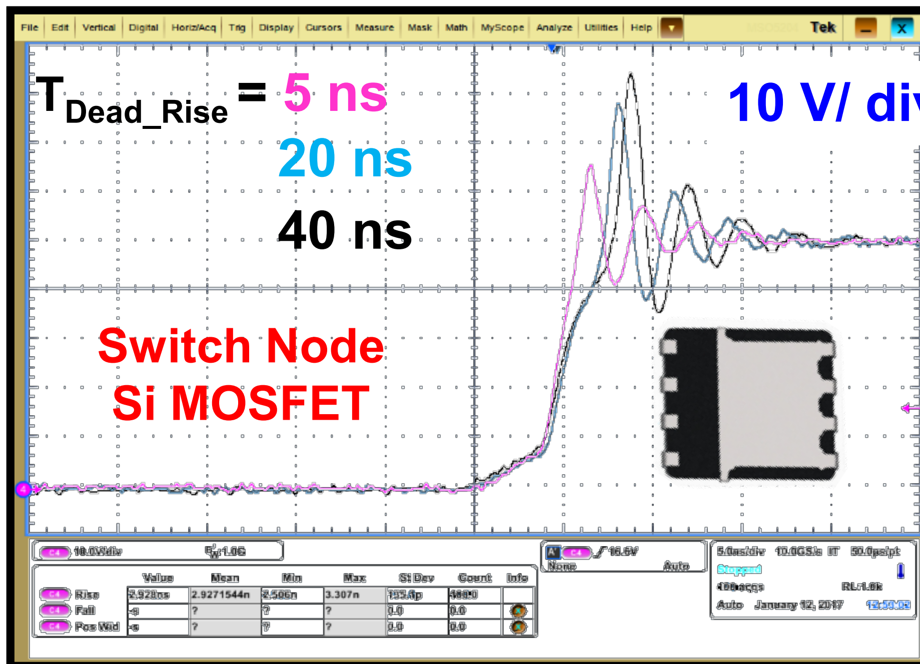
Like a MOSFET but…

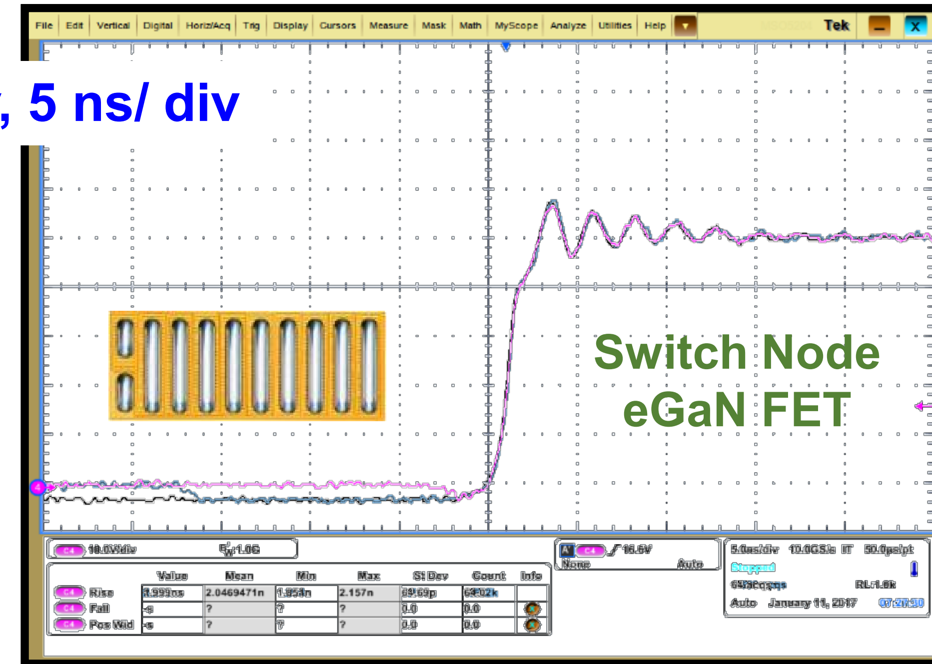
- Smaller
- Switches fast
  - Lower FOM's
- Reverse voltage conduction
- Zero reverse recovery (Q_{RR})
- Miller ratio < 1 (Q_{GD}/Q_{GS_Th})
  (dv/dt immunity)
- Exceptional reliability



GaN FETs have Zero Reverse Recovery

- Higher hard-switching frequencies without penalty
- Lower switching distortion

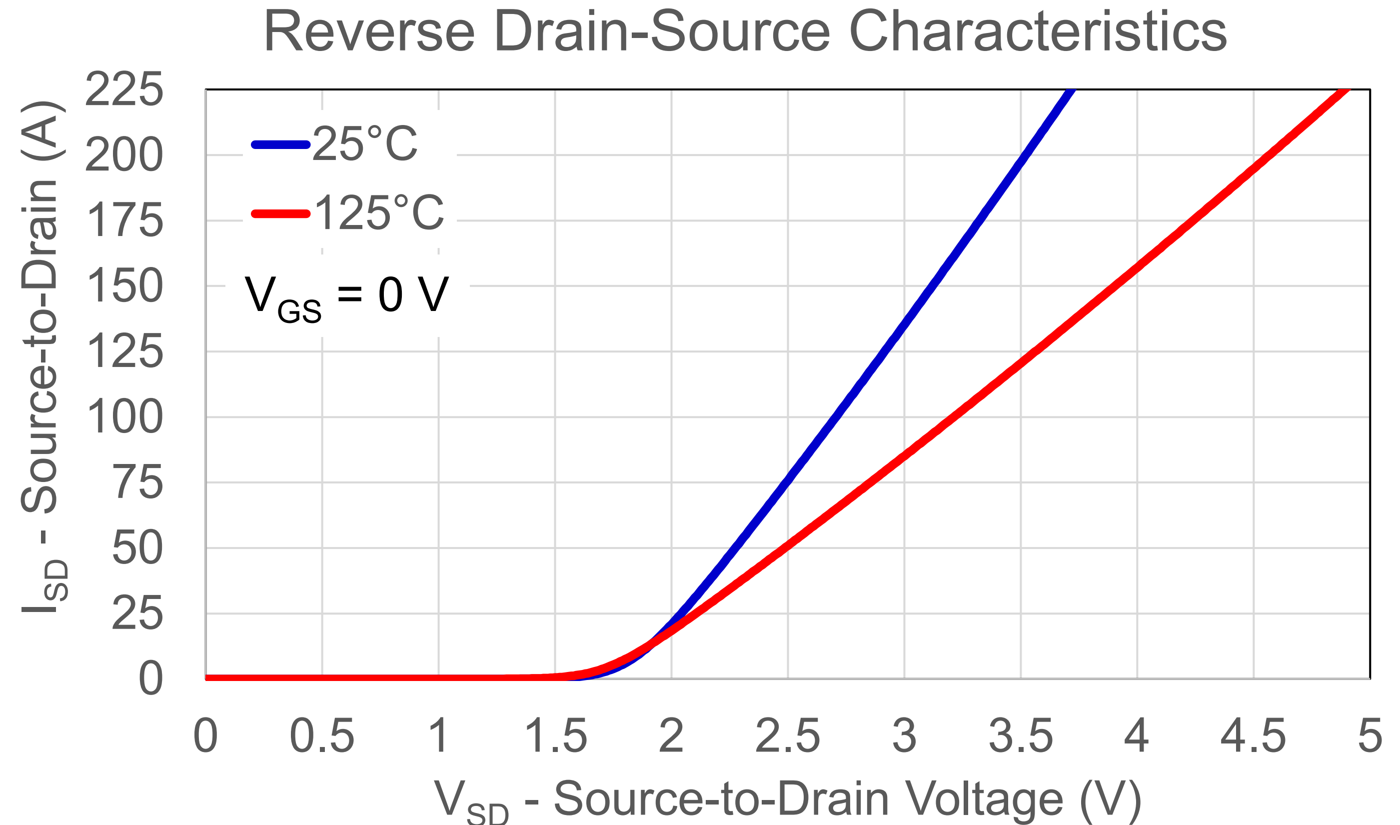




V_{IN} = 48 V, V_{OUT} =12 V, I_{OUT} = 20 A, f_{sw} = 500 kHz, L_{Buck}= 4.7μH

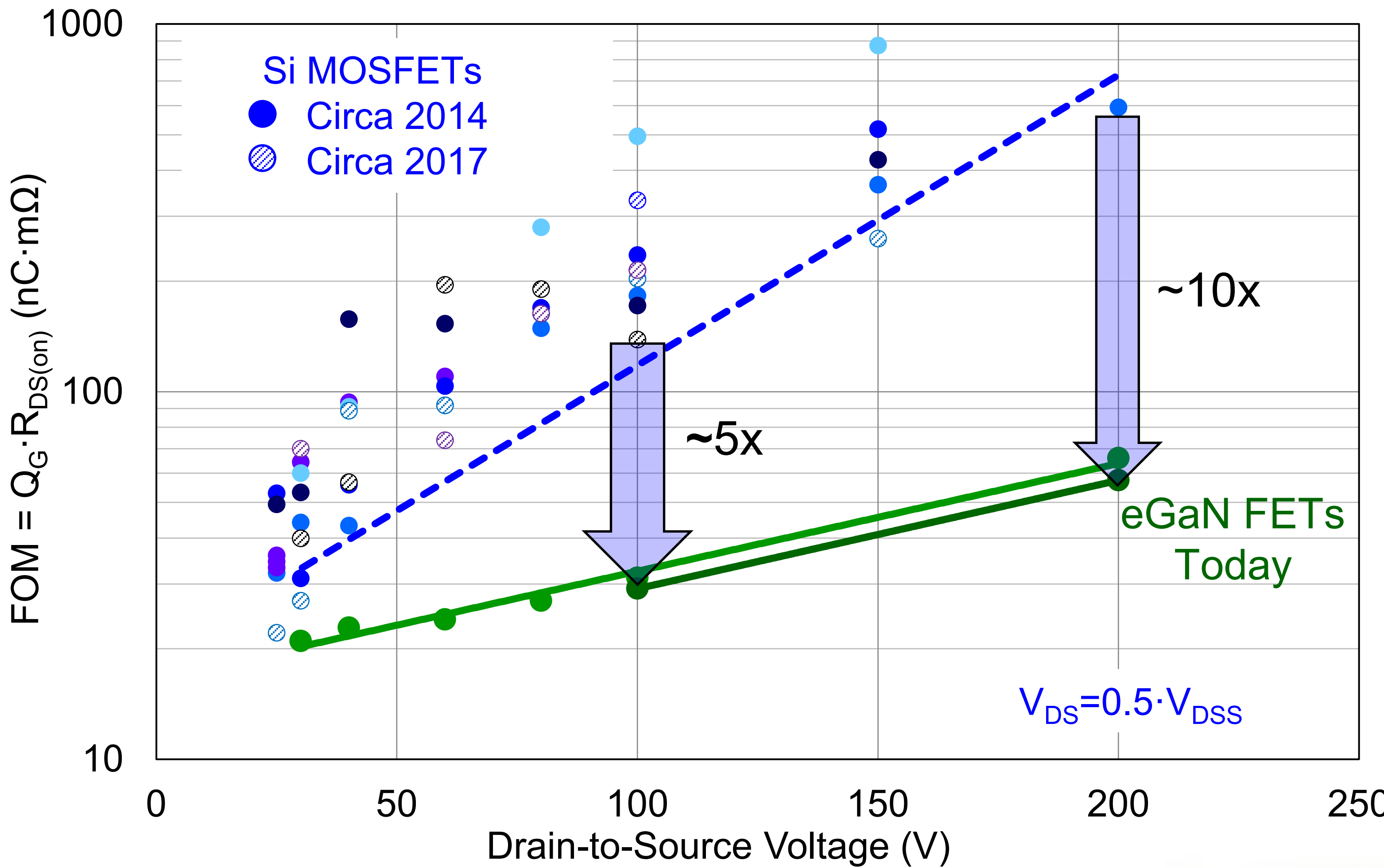
GaN FET Reverse Conduction

- Higher than MOSFETs
- Behaves like a diode
- Easy to manage
    - Dead time
    - Anti-parallel diode



Switching Characteristics

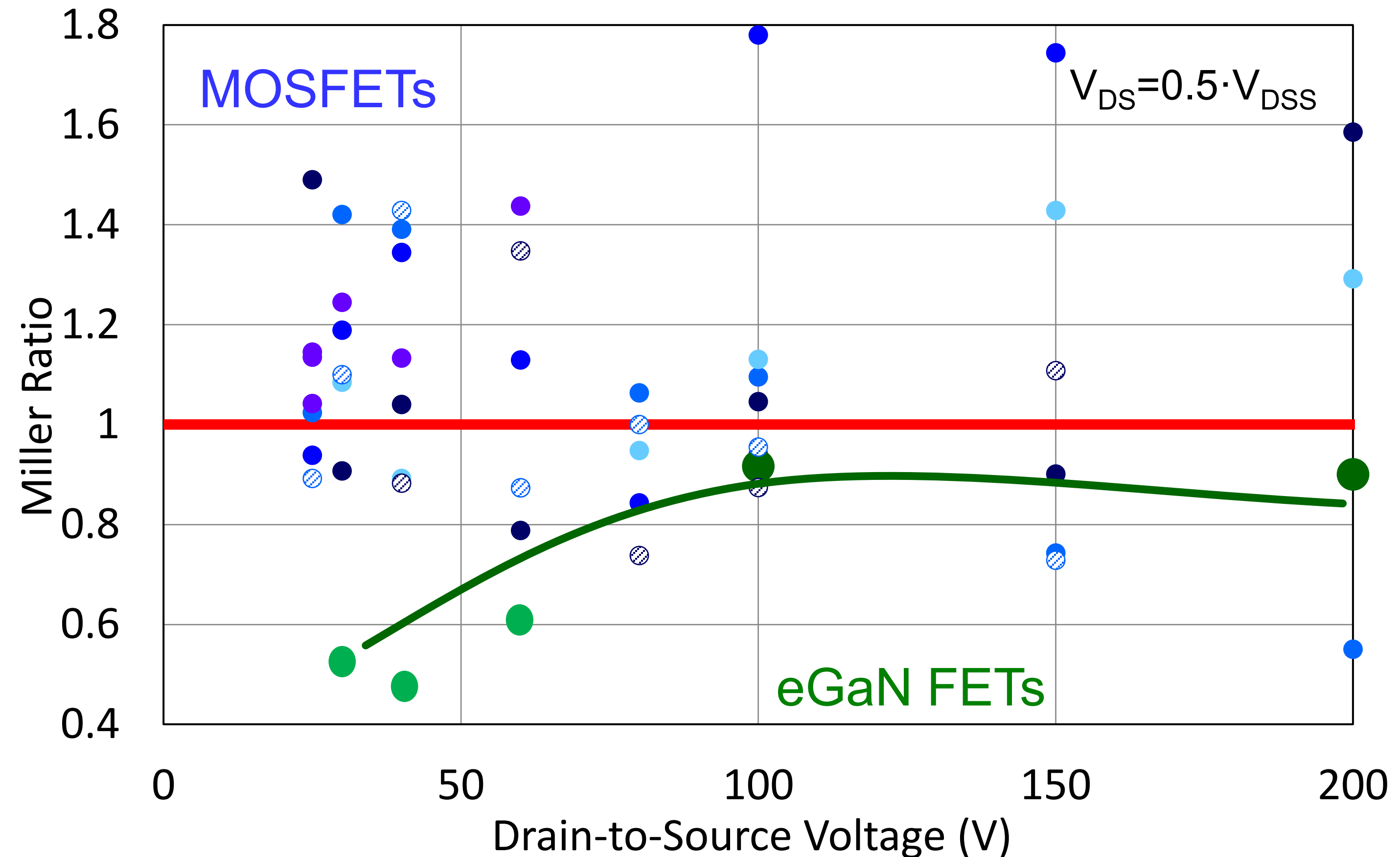
GaN FETs switch much faster than MOSFETs



Miller Ratio

$$Ratio_{Miller} = \frac{Q_{GD}(V_{DS})}{Q_{GS_Th}}$$

- Indicator of dv/dt immunity
  - Simplifies gate driver requirements
  - Reduces converter startup failures
- GaN FETs Miller ratio across full rated voltage



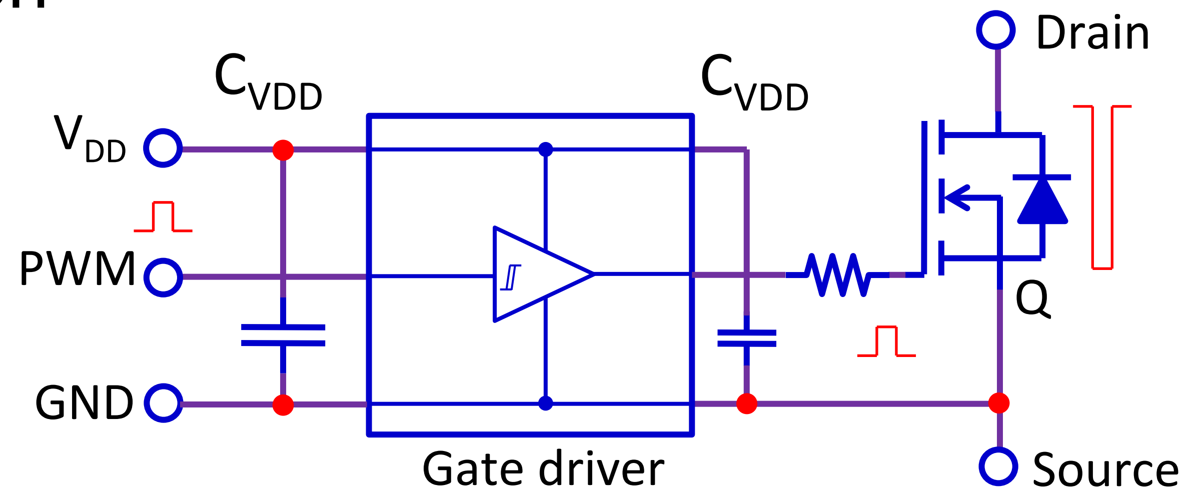
Designing with GaN FETs

- Gate drivers
- Layout techniques and the importance of inductance
- Overview of the PCB based thermal system
- Adding a heatsink to GaN Devices

GaN FET Gate Drivers

Gate driver interfaces the PWM to the FETs

- Critical to reliable converter operation
- Driving requirements
- Protection features
- Timing requirements
- GaN FET specific requirements

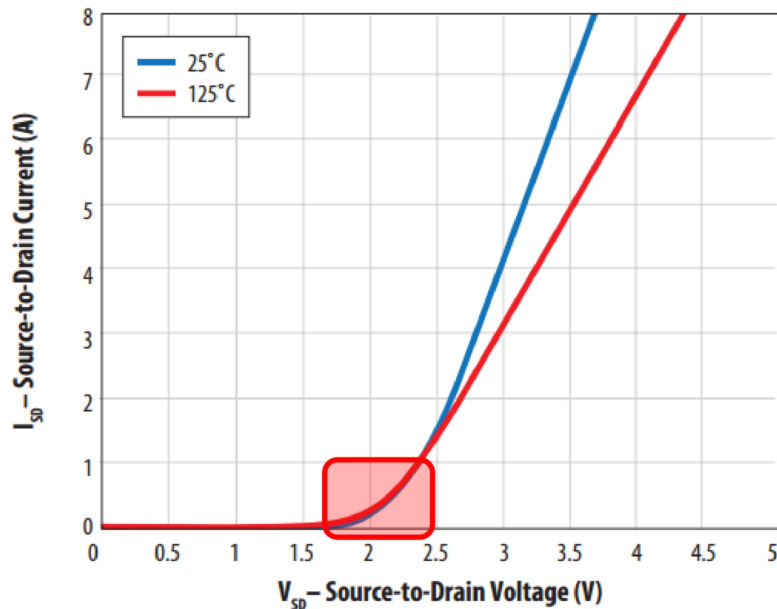


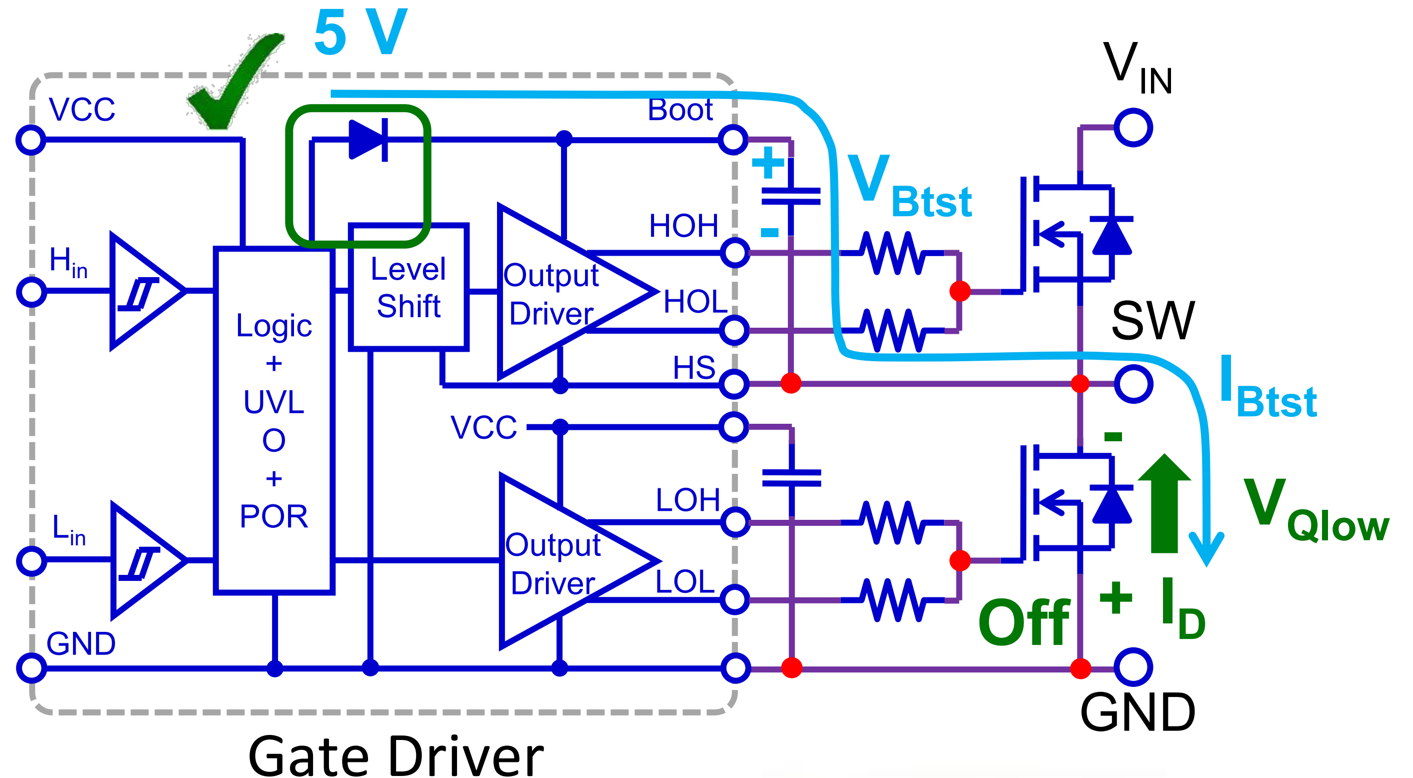
Dead-time and Reverse Conduction

GaN FET reverse conduction voltage ≈ 2.5 V

- Driver must include bootstrap over-voltage management
- Driver must work with negative switch-node voltage up to 5 V

$V_{Btst} = 5\text{ V} - V_{Qlow} \approx 7.5\text{ V}$

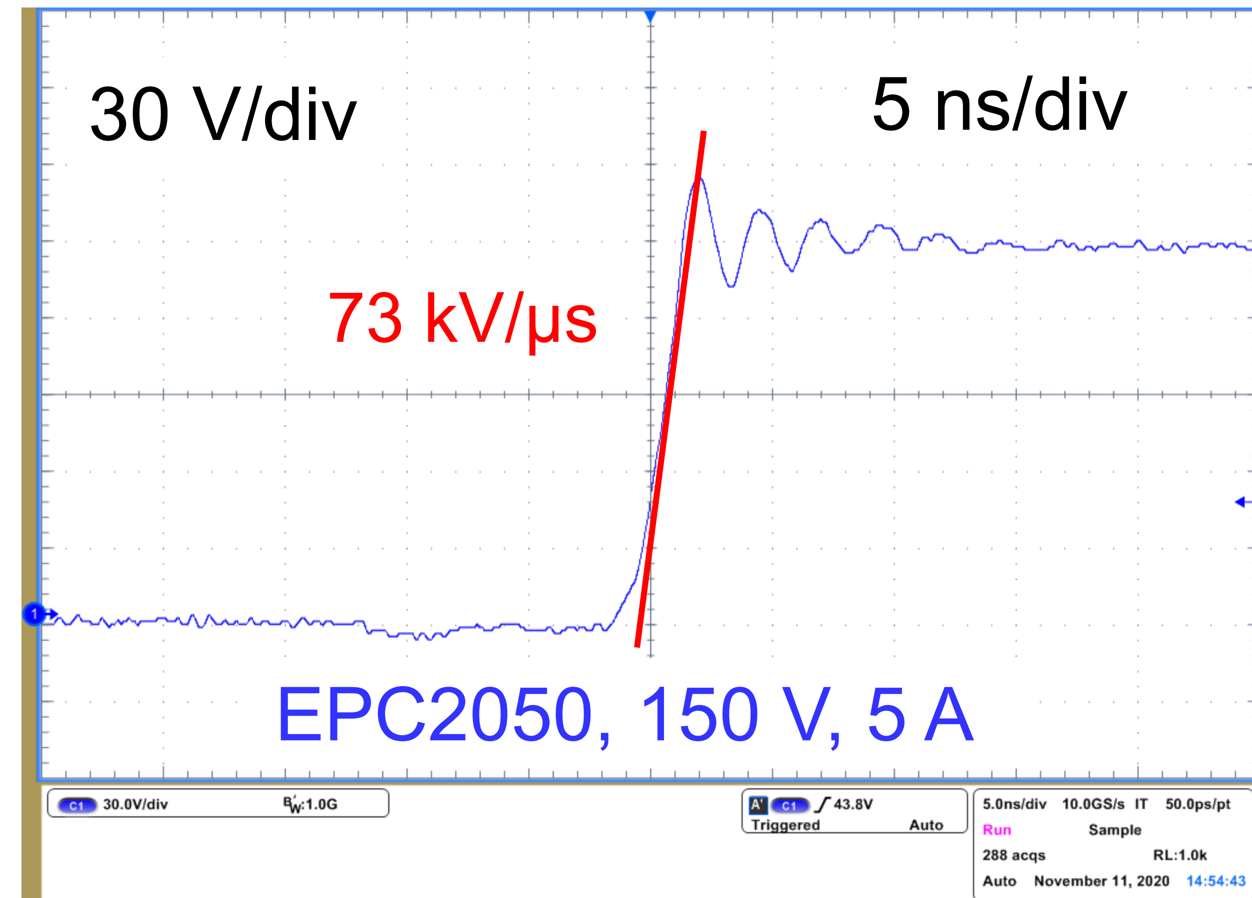




Required Driver dv/dt Capability

GaN FETs switch fast

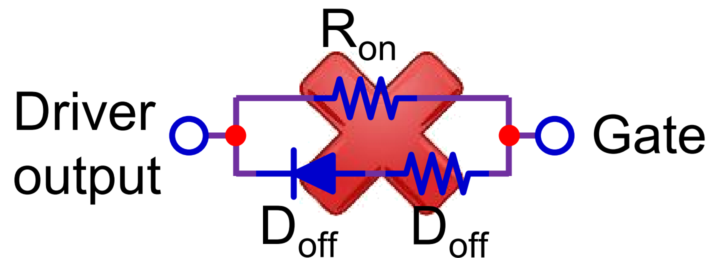
- Applicable to half-bridge drivers
- Driver should be rated >100 kV/µs
- Higher voltage rated FETs switch faster
- Increasing gate resistances reduces dv/dt
  - Efficiency penalty

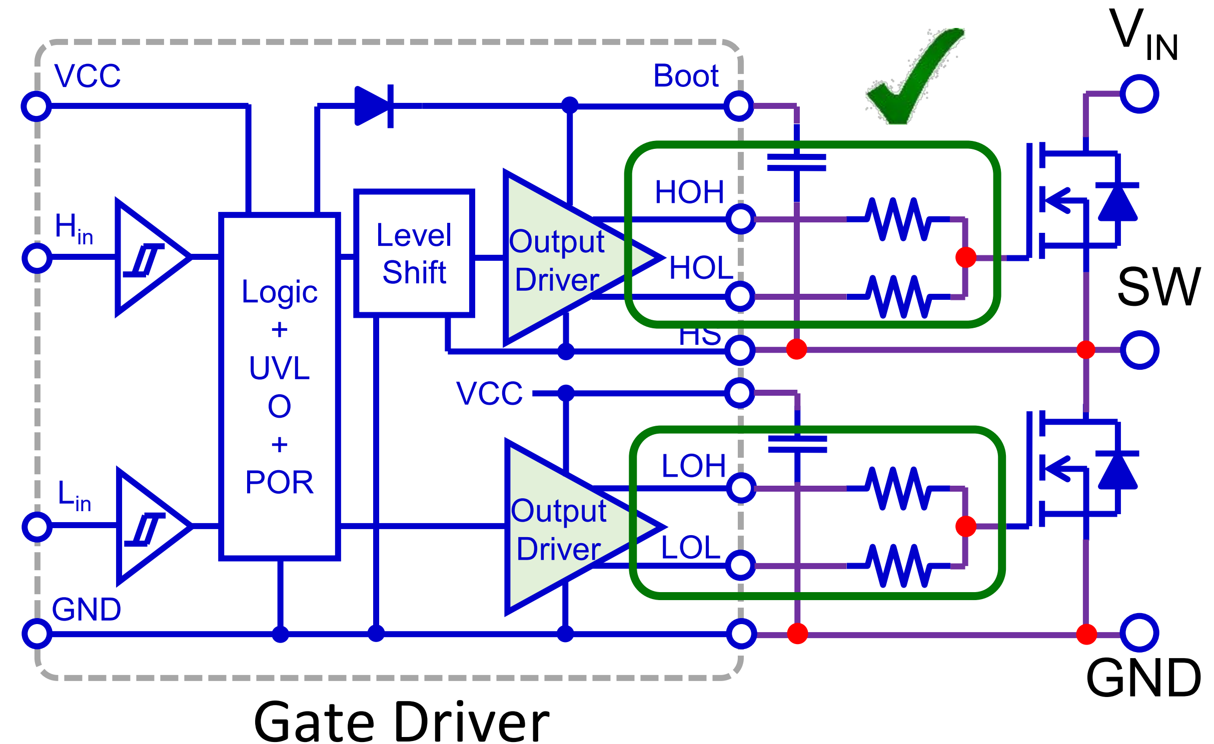


Driving GaN FET Threshold Voltage

GaN FETs have low $V_{TH} \approx 0.7\ V – 1.5\ V$

- Ensure good off state
- For optimum performance use drivers with separate turn-on and turn off gate connections
- Avoid circuit below for single output gate drivers

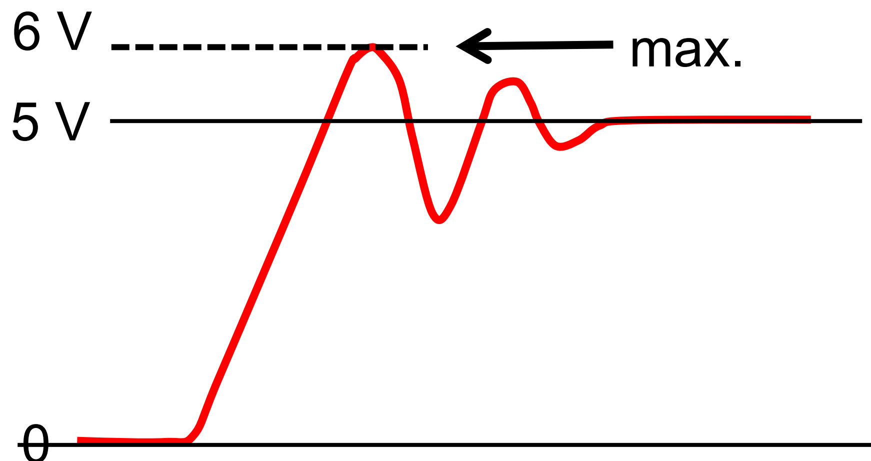


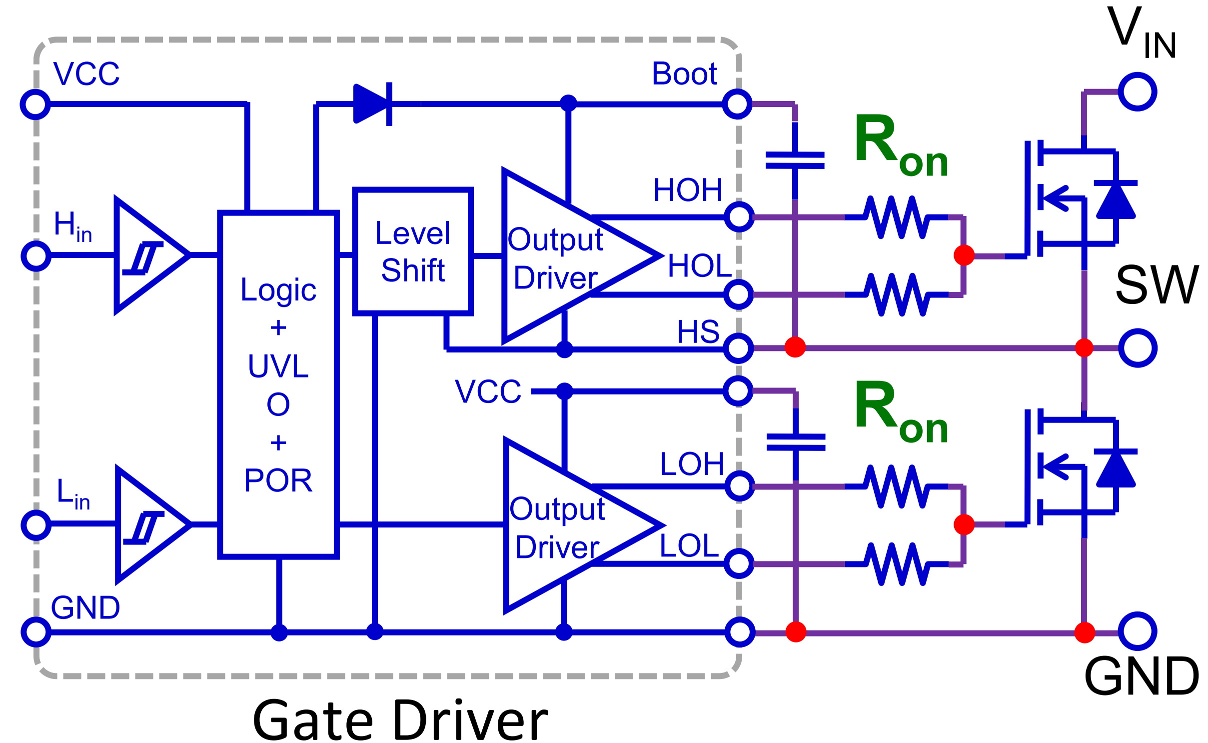


GaN FET Gate Over-Voltage Management

Max. V_{GS} = 6.0 V

- Above limit affects reliability
- Drive gate with 5 V
- Damp ringing with resistor (R_{on})
  - Gate loop inductance (L_{Gon})
  - Common-Source inductance (L_{CSI})
  - Gate Capacitance (C_{GSon})





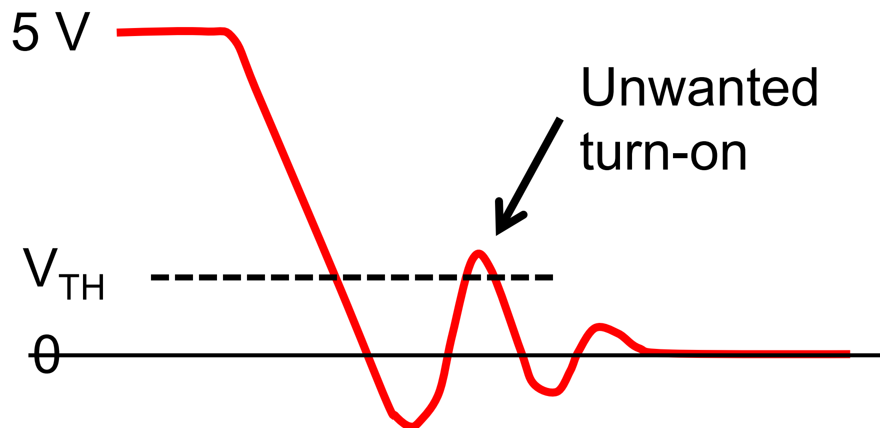
Gate Driver

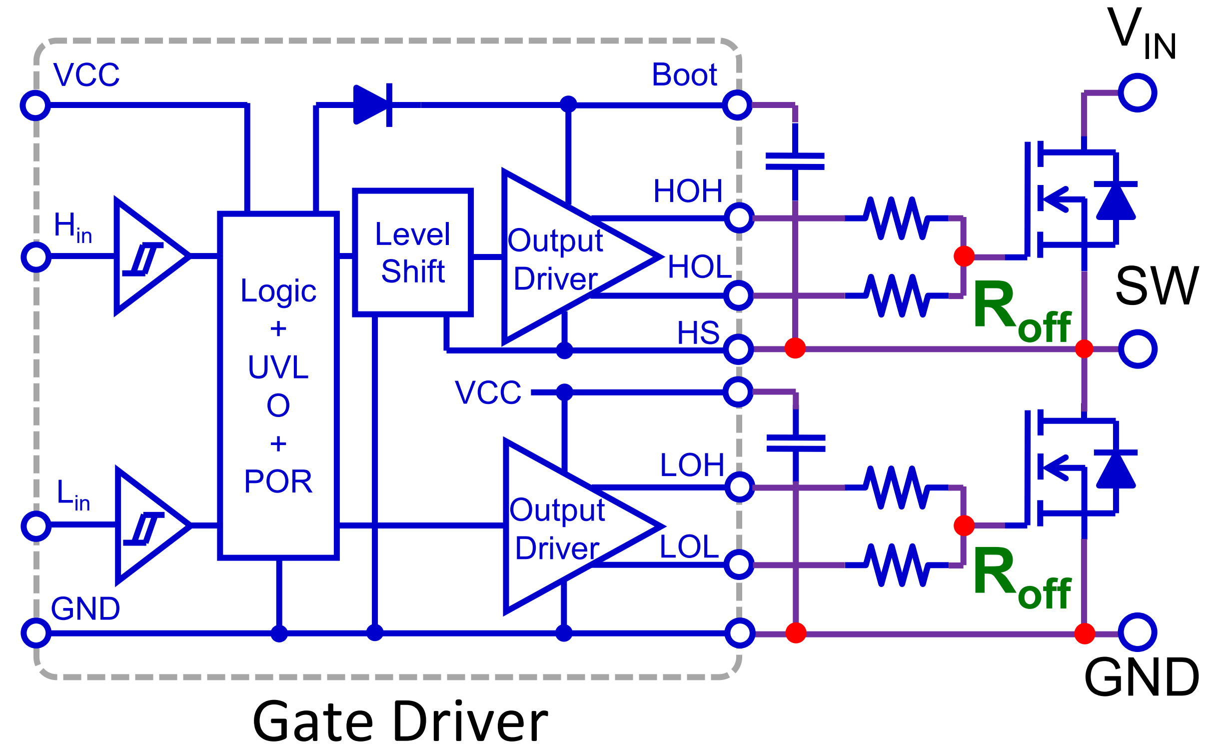
$$R_{on} \geq \sqrt{\frac{4 \cdot (L_{Gon} + L_{CSI})}{C_{GSon}}}$$

GaN FET Gate Under-Voltage Management

Prevents ringing-based turn-on when FET was turned off

- Damp ringing with resistor (R_{off})
  - Gate loop inductance (L_{Goff})
  - Common-Source inductance (L_{CSI})
  - Gate Capacitance (C_{GSoff})



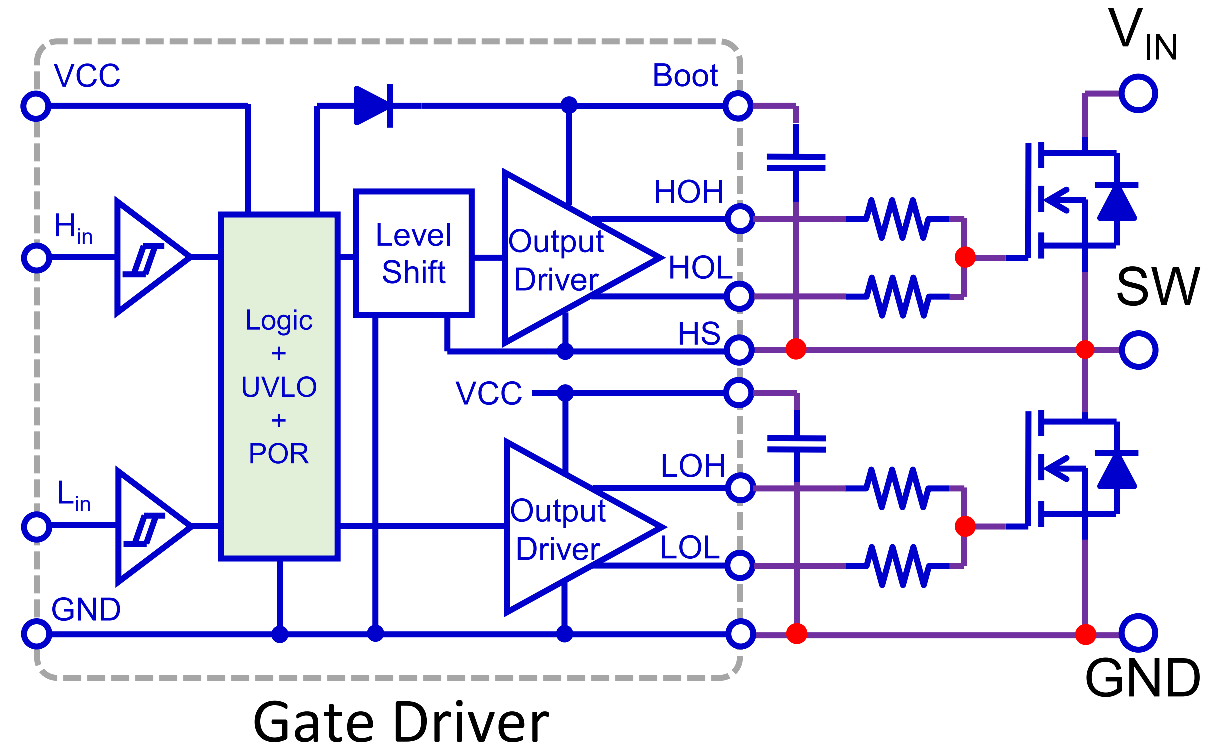


$$R_{off} \geq \sqrt{\frac{4 \cdot (L_{Goff} + L_{CSI})}{C_{GSoff}}}$$

Under-Voltage Lockout

Prevents gate turn-on when driver supply voltage is too low

- Min. recommended GaN FET thresholds:
  - 4.0 V enable
  - 3.8 V disable
- Applies to both upper and lower FET drivers

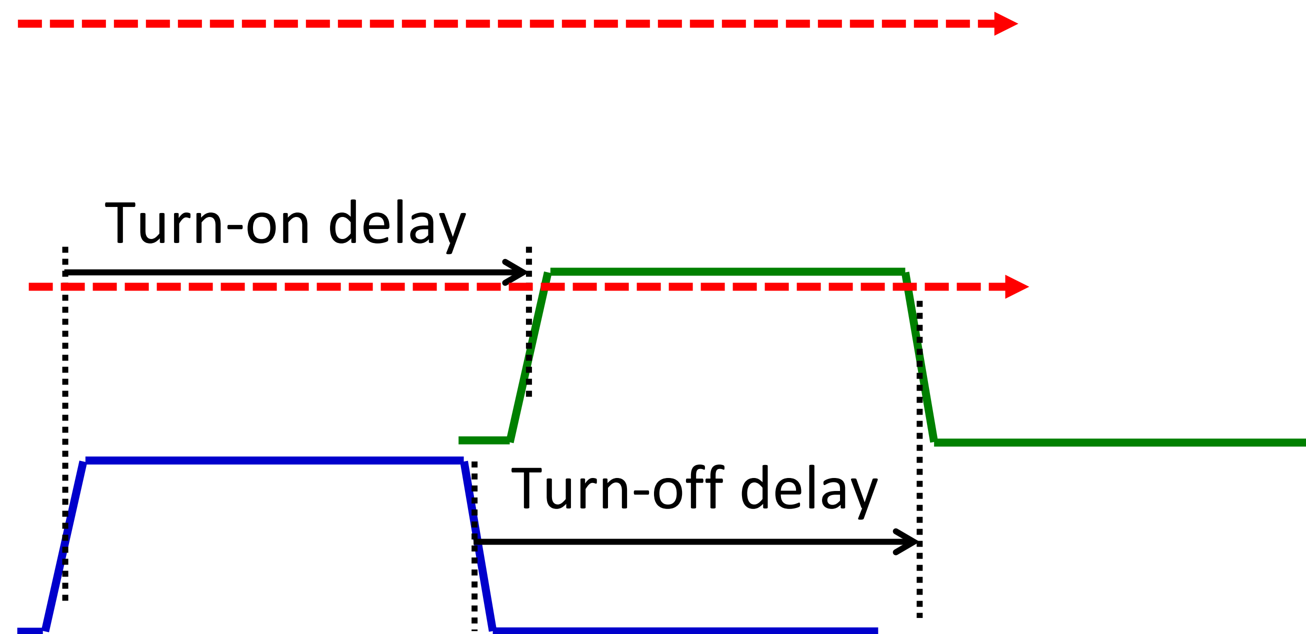


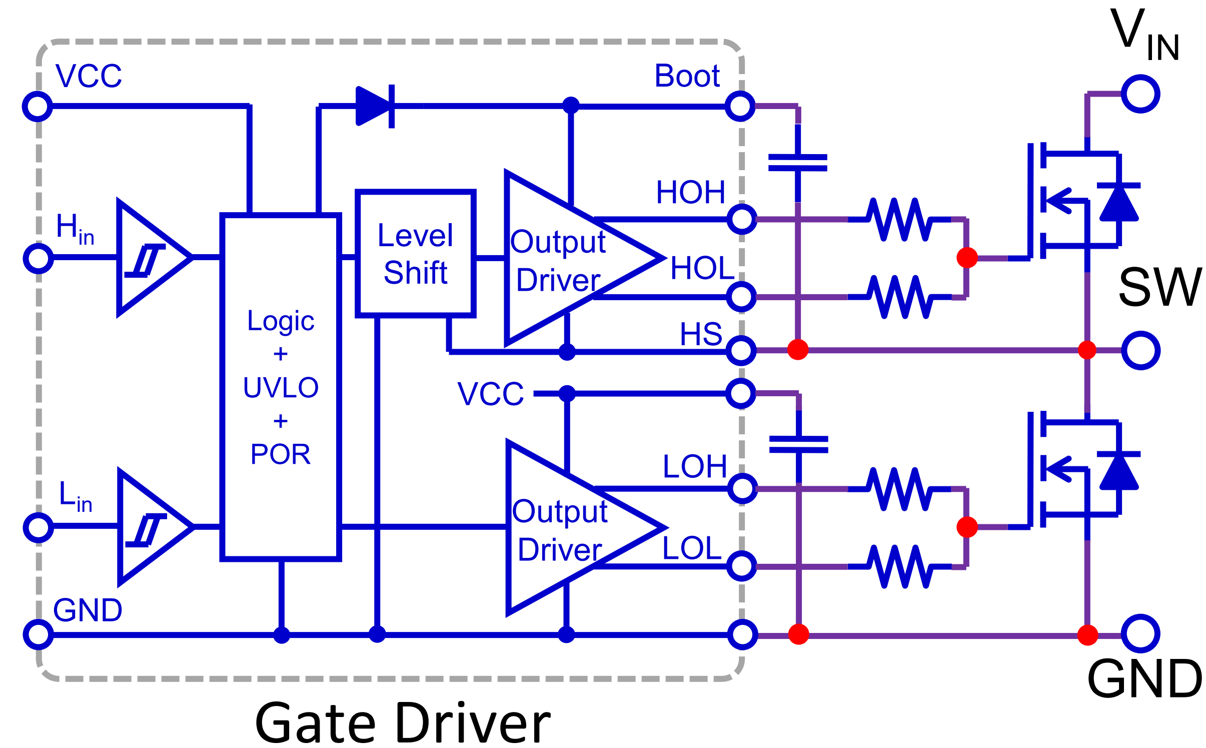
Gate Driver

Propagation Delay and Matching

Input signal to gate output delay

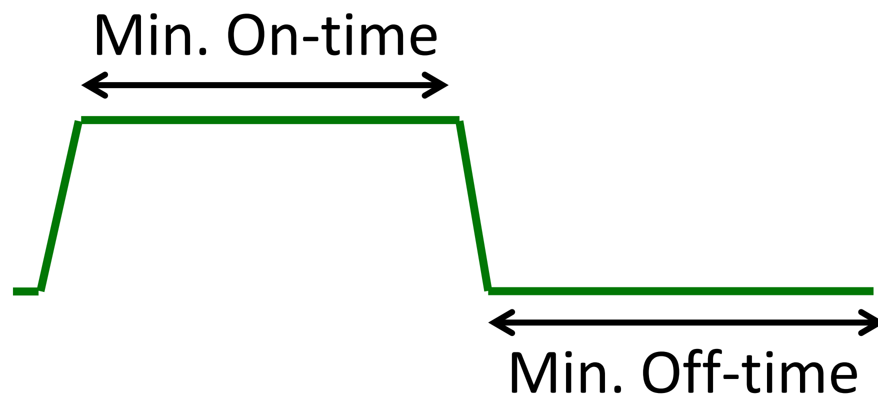
- On/Off delays should be matched within 5 ns
- Max. delay should be limited to 50 ns

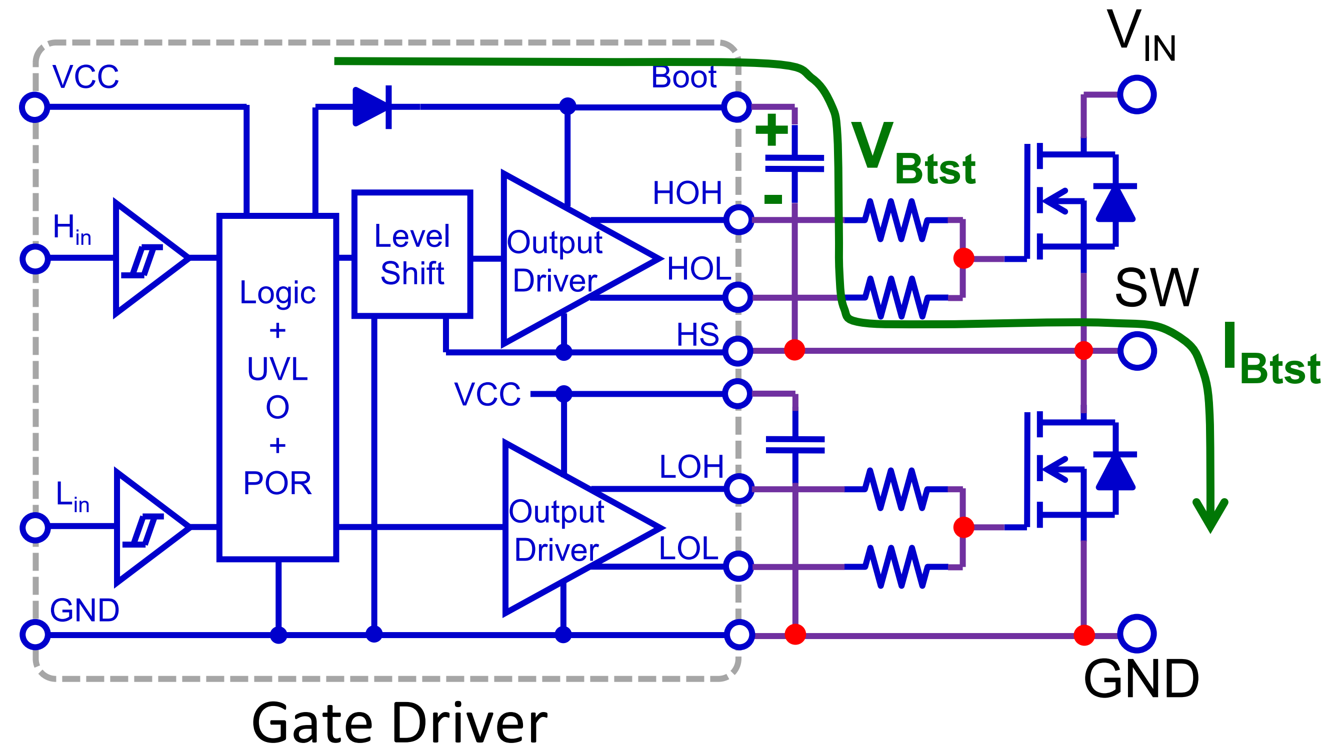




Minimum Pulse Width

- Ensures proper turn-on and -off
  - Within the gate driver
  - Within the power circuit
- Allows proper bootstrap charging





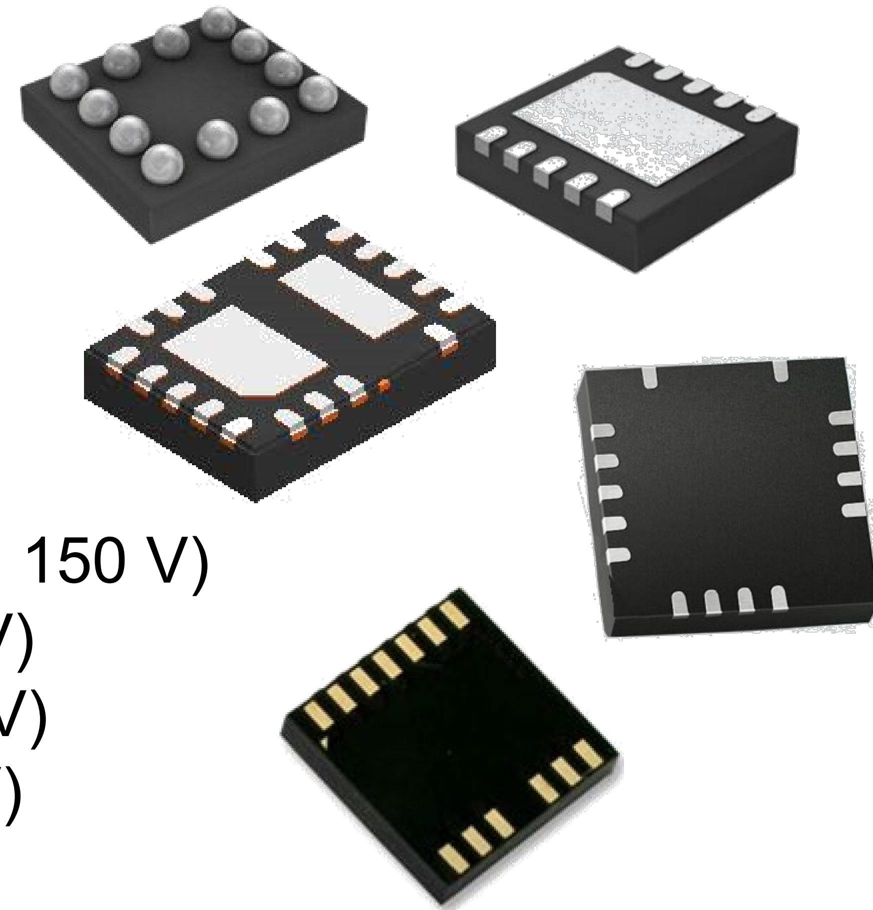
GaN Compatible Gate Drivers

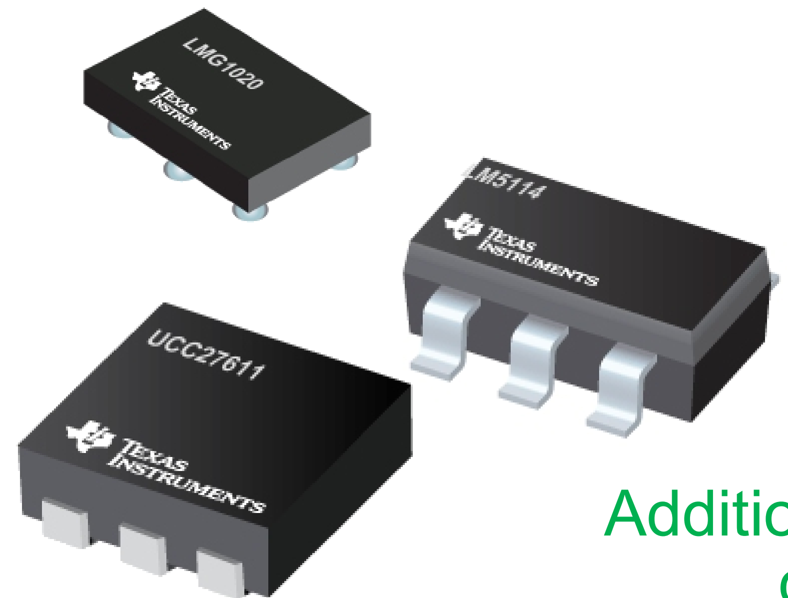
Single Drivers

- LMG1020 & -25[a] : Ultra fast
- UCC27611 – with LDO
- LM5114 - Standard

Half Bridge Drivers

- LMG1205‡ (90 V)
- uP1966E‡ (80 V)
- MP8699B ‡ (100 V)
- LM5113-Q[a] (100 V)
- MPQ1918[a] (100 V)
- LMG1210 (200 V)
- NCP51820 & -10 (650, 150 V)
- STDRIVEG600 (600 V)
- Si827xGB1-IM*[a] (650 V)
- ADuM4221A * (>600 V)





Additional Gate drivers in development

*isolated ‡ Footprint compatible
[a] automotive

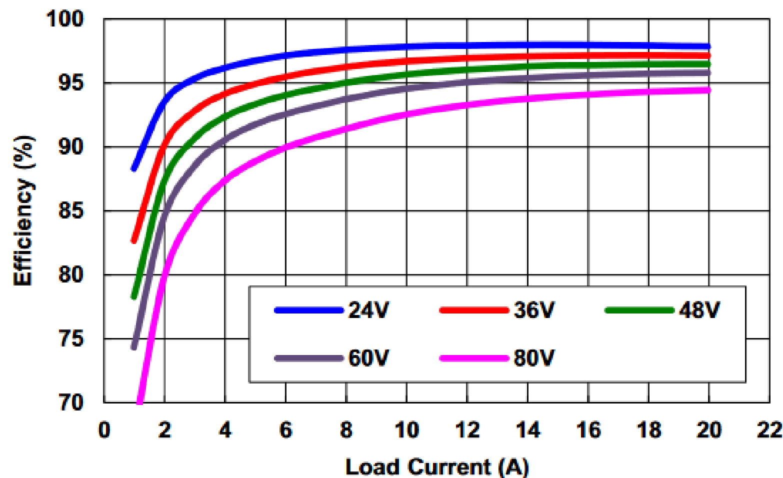
GaN Compatible Controllers

Single Buck Controller

- LTC7891   input 5-100 V, 0.1-3 MHz
  - Example design at 2 MHz

Dual (or 2-phase) Buck Controller

- ISL81806 input 5-80 V, 0.1-2 MHz
  - Example Design: EPC9157



Dual (or 2-phase) Boost Controller

- ISL81807   output up to 80 V, 0.1-2 MHz
  - Example Design: EPC9166

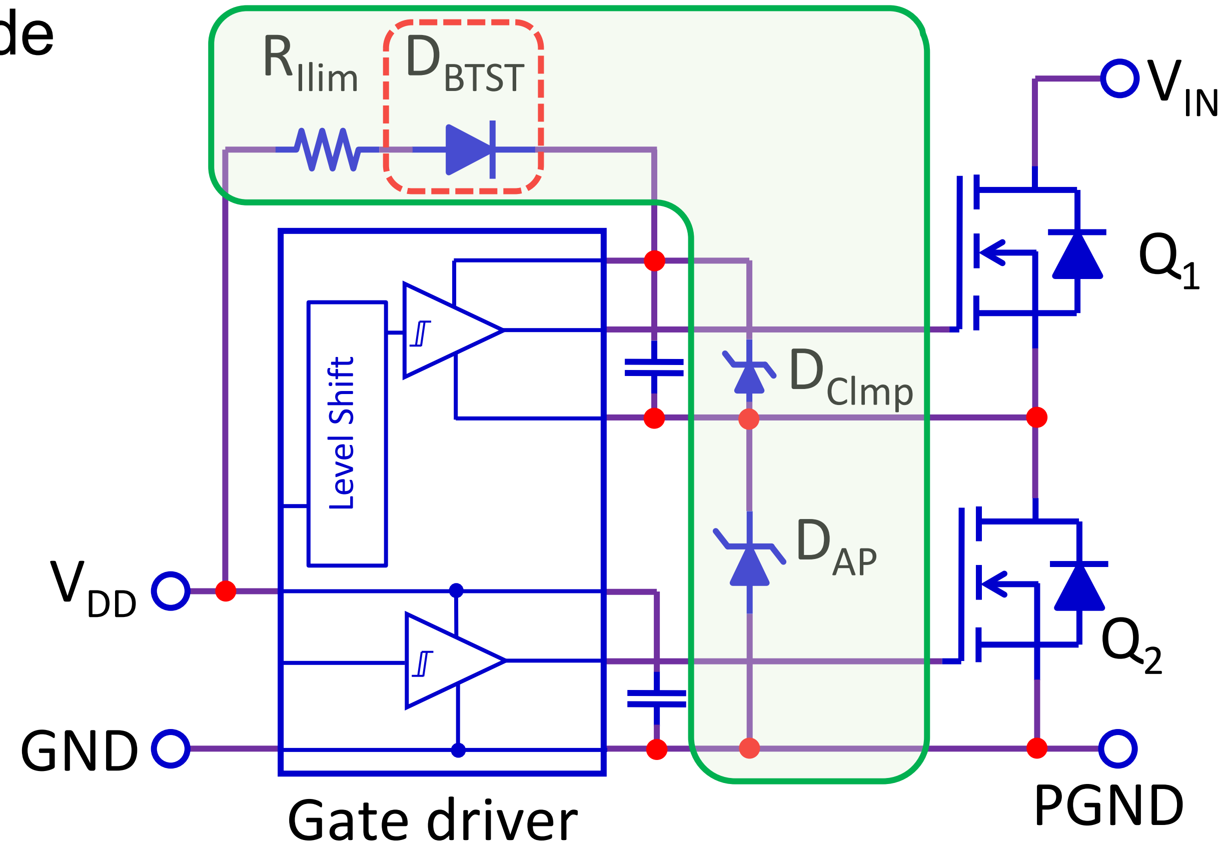
Synchronous Rectifier Controller

- Several available, see list

Additional GaN Controllers in development

Adapting MOSFET Drivers for GaN FETs

- Driver MUST use an external bootstrap diode (D_{BTST})
- Ensure UVLO & operating voltage match GaN FET gate
- Add measures to prevent bootstrap over-charging
  - Add 5.2 V Zener clamp (D_{Clmp})
  - Add series current limit resistor (R_{Ilim})
  - Schottky anti-parallel diode (D_{AP}) (where applicable), mostly low voltage

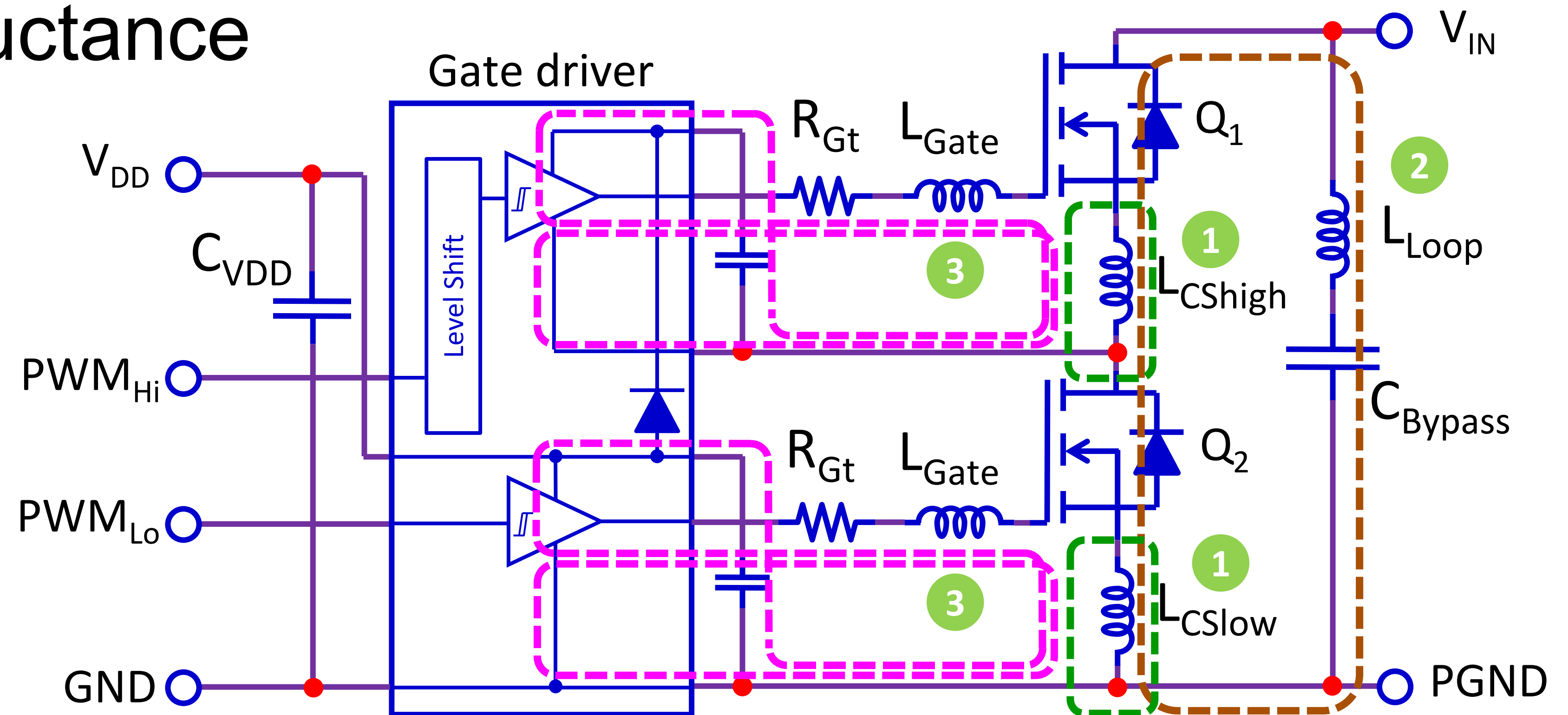


High Performance Layout Techniques

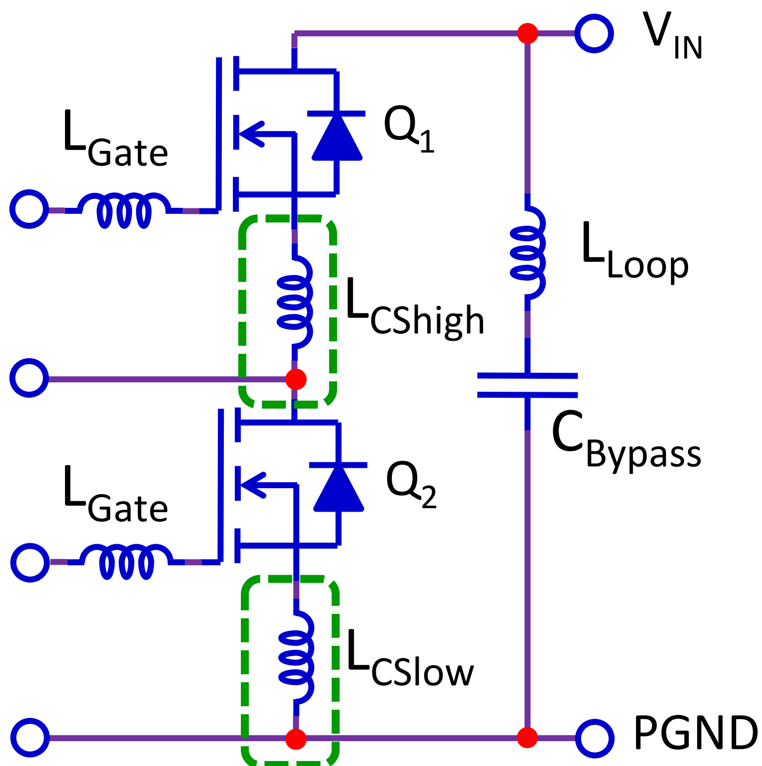
- Parasitic Inductances and their Impact on Converter Performance
- Layout Design Comparisons
- Designing a Low Inductance Layout
- Alternative Layout Configurations
- Gate Circuit Layout
- Working with Single IC Dual Gate Drivers
- Considerations to Add a Source Shunt

Parasitic Inductance Considerations

1. Common source inductance
2. Power loop inductance
3. Gate loop inductance
   - Turn-on
   - Turn-off



Impact of Common Source Inductance



V_{IN}=12 V, V_{OUT}=1.2 V,
f_{sw}=1 MHz, I_{OUT}= 20 A

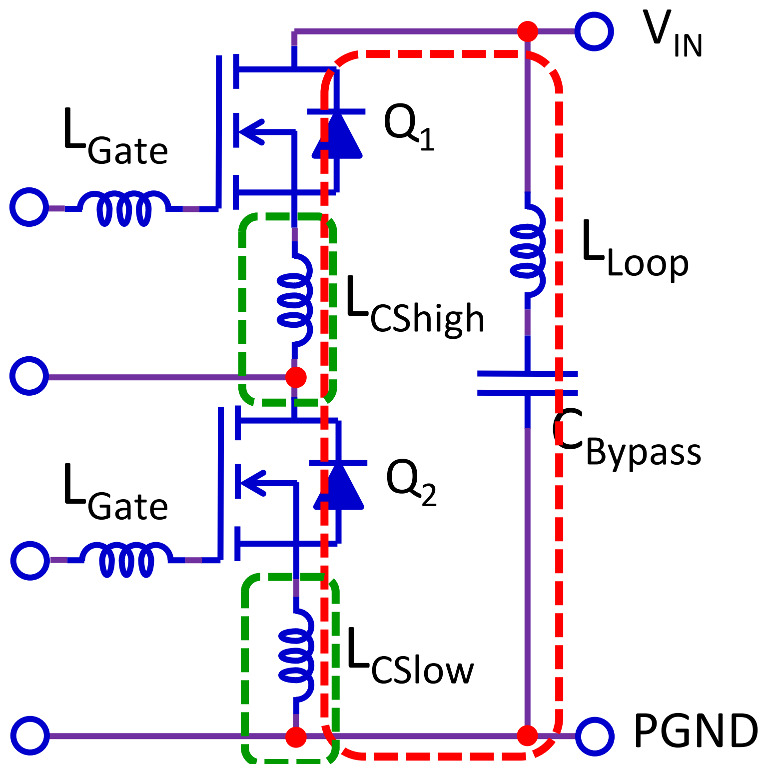
Power Loss[W]

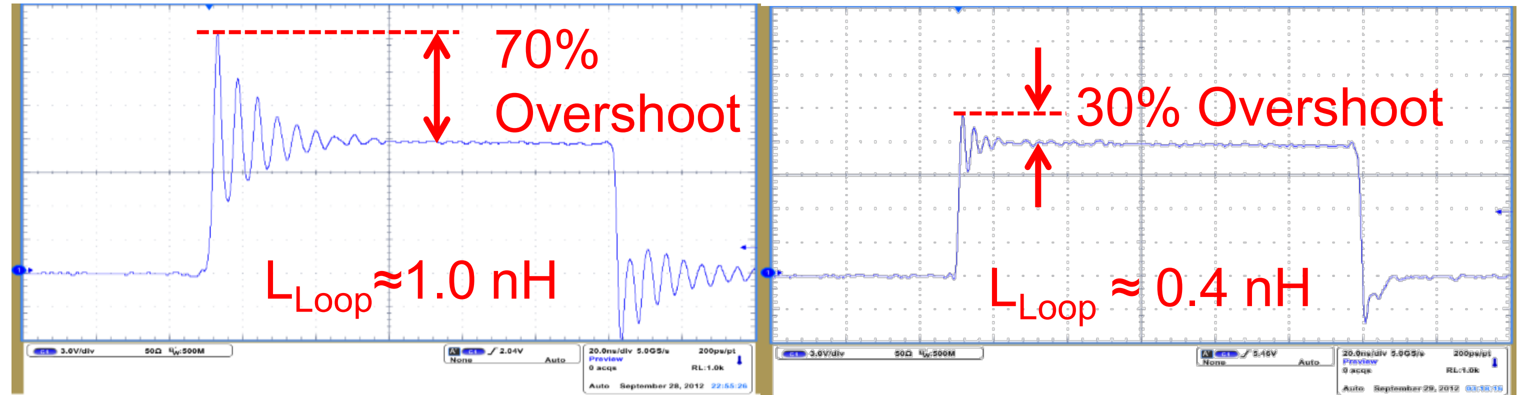
5.5
5.0
4.5
4.0
3.5
3.0

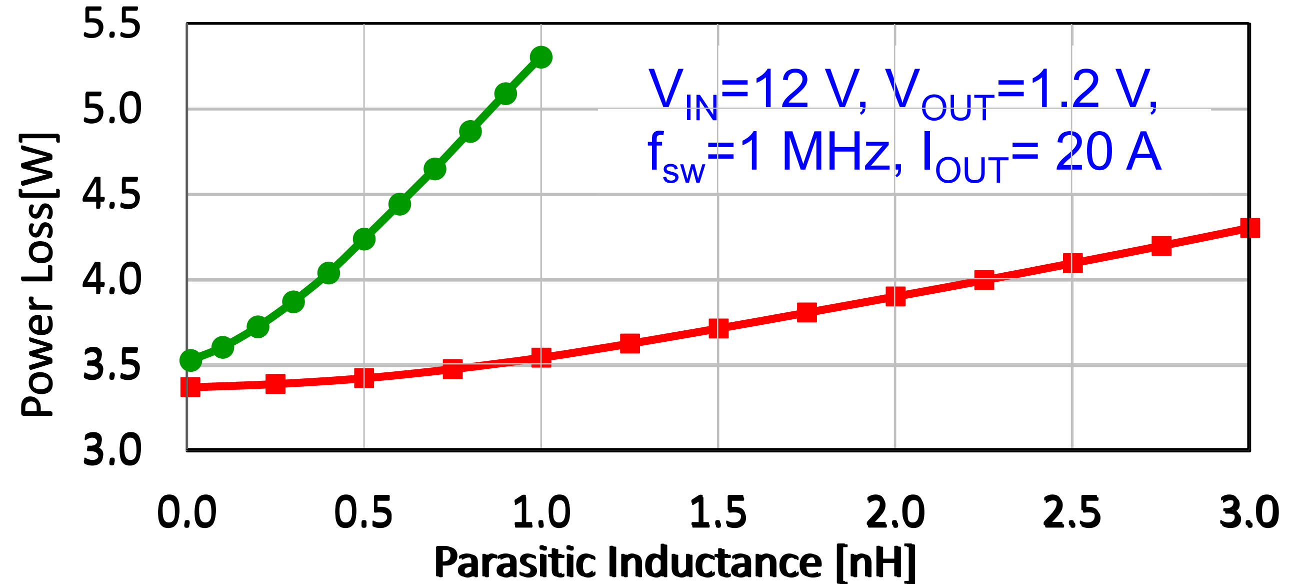
0.0 0.2 0.4 0.6 0.8 1.0

Parasitic Inductance [nH]

Impact of Power Loop Inductance

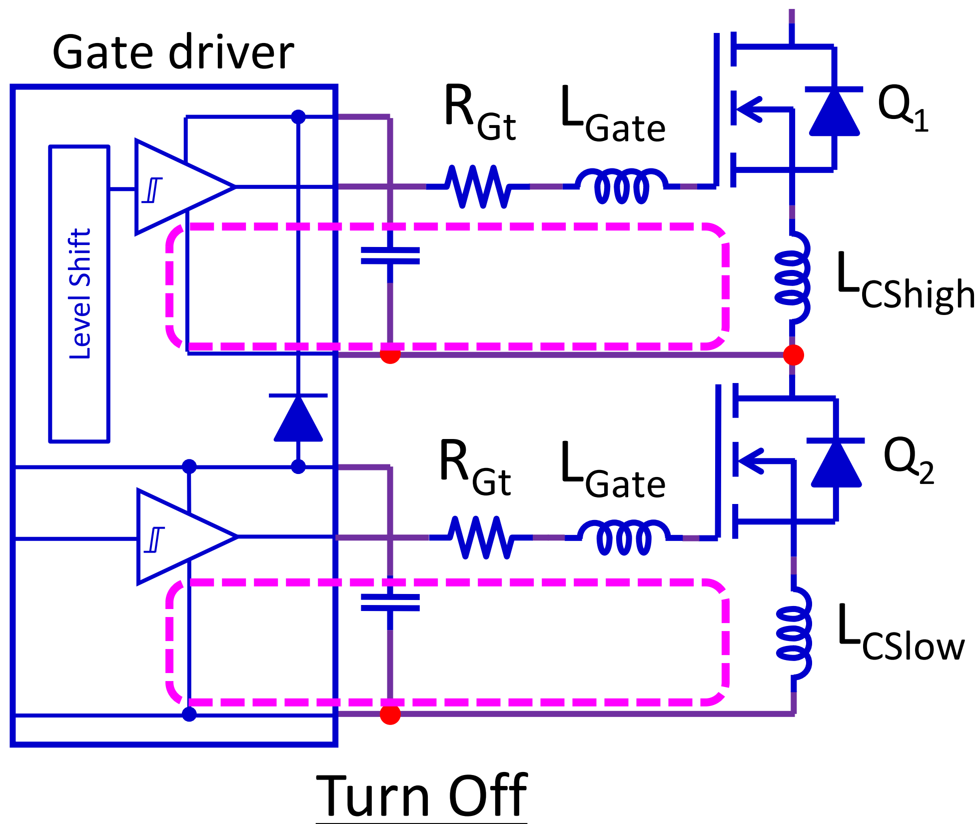


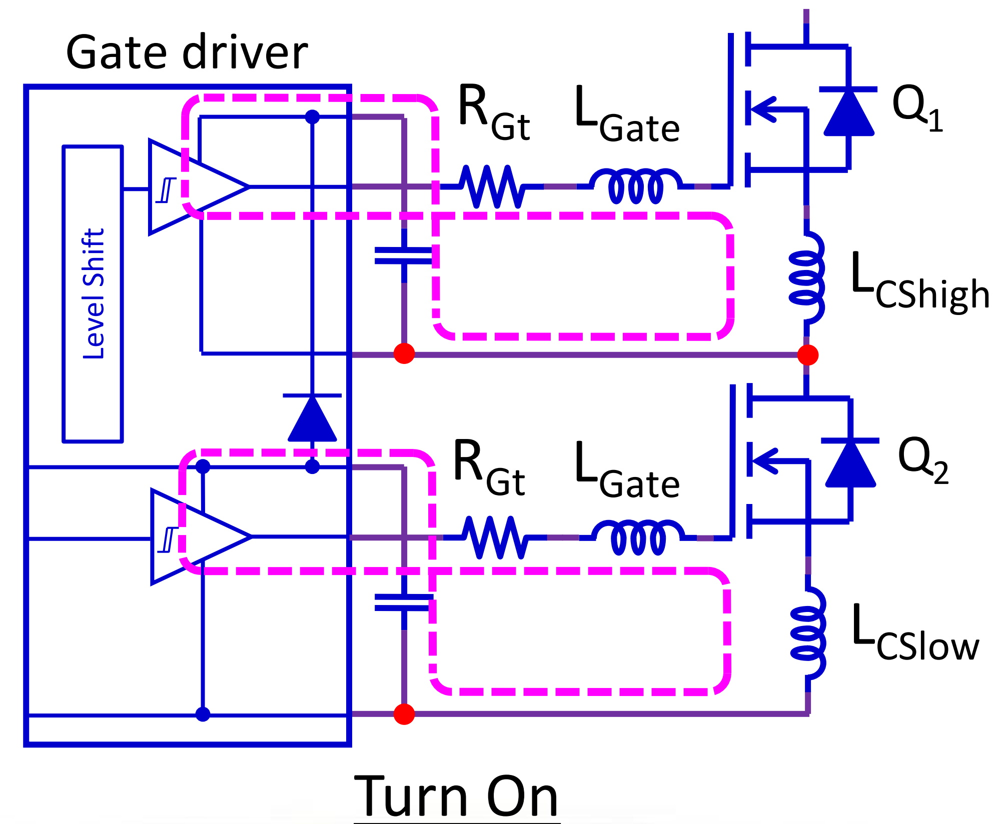




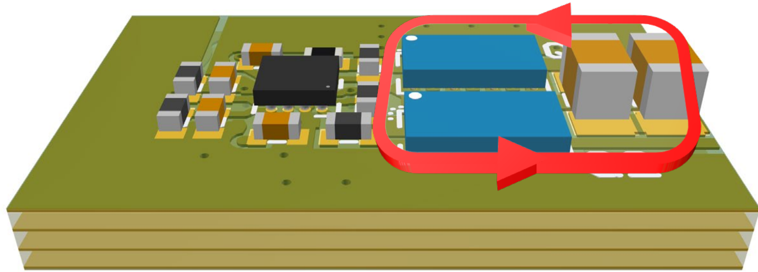
Impact of Gate Loop Inductance

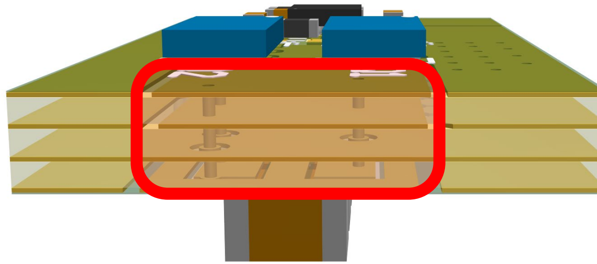
- Two loops to consider: Turn-on & Turn-off
- L_{Gate} requires R_{Gt} to damp ringing overshoot
  - slows transition

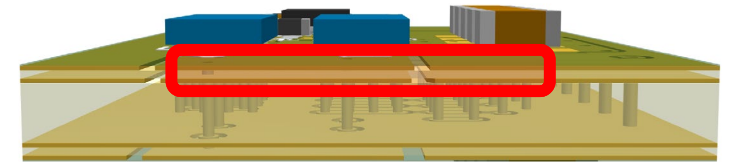


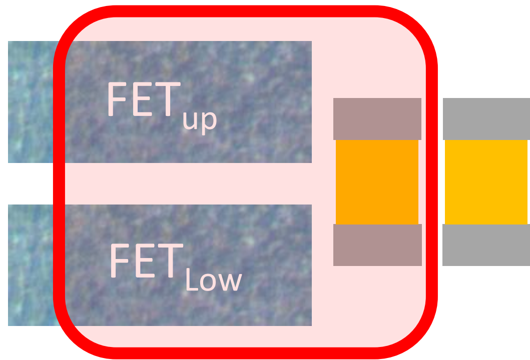


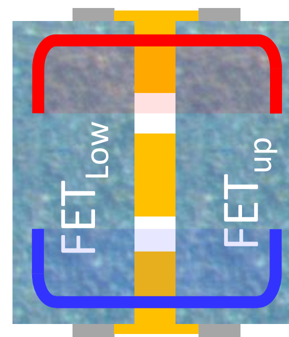
Layout Comparisons

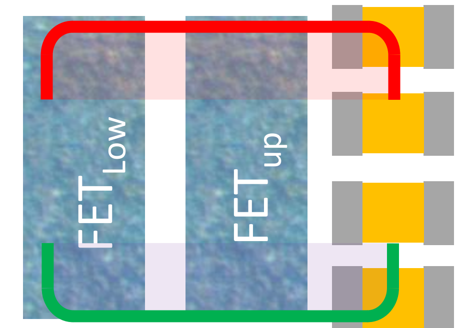












Top Layer

Top Layer Bottom Layer

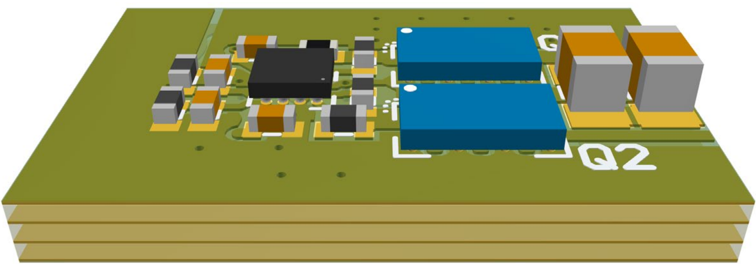
Top Layer Inner Layer 1

Lateral

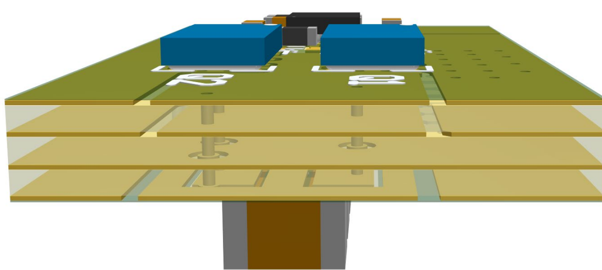
External Vertical

Internal Vertical

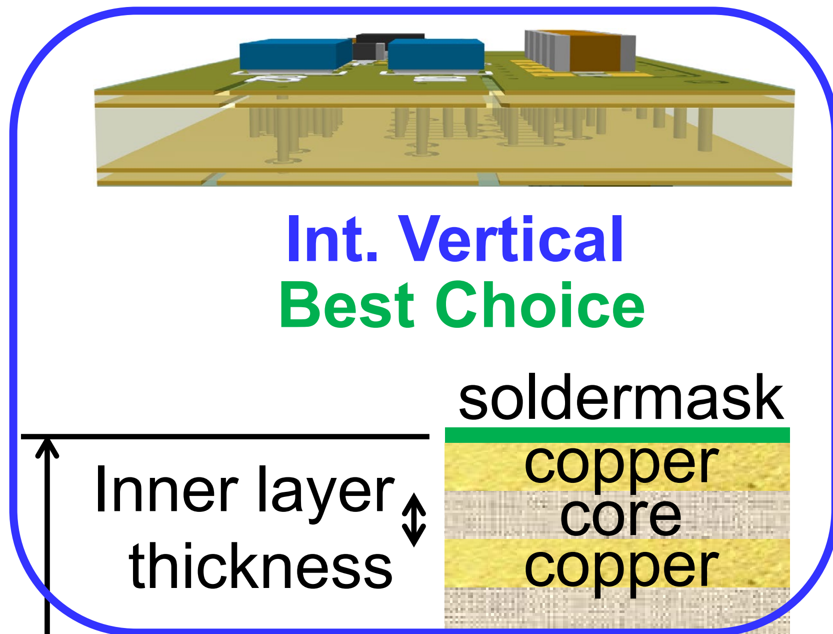
Layout Inductance Comparison



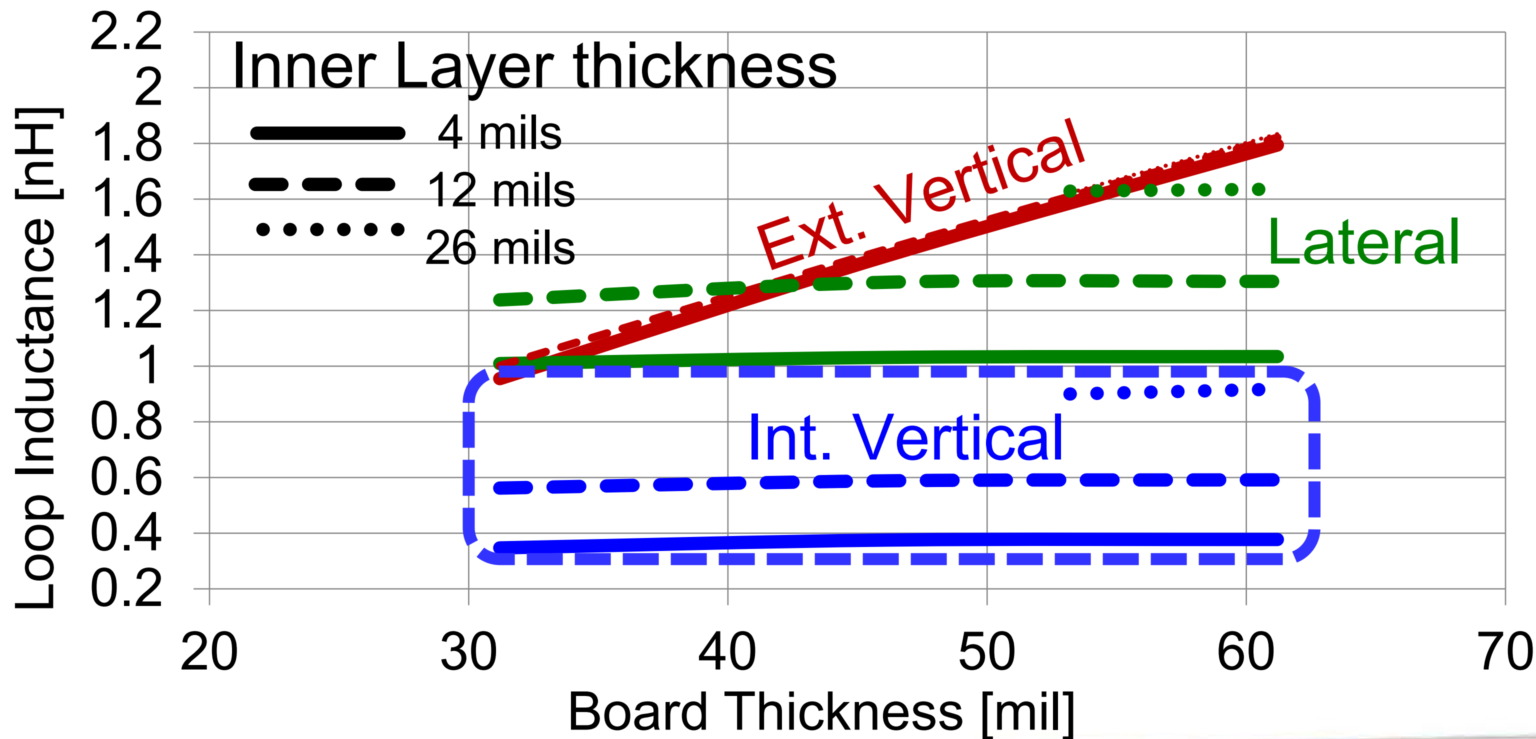
Lateral

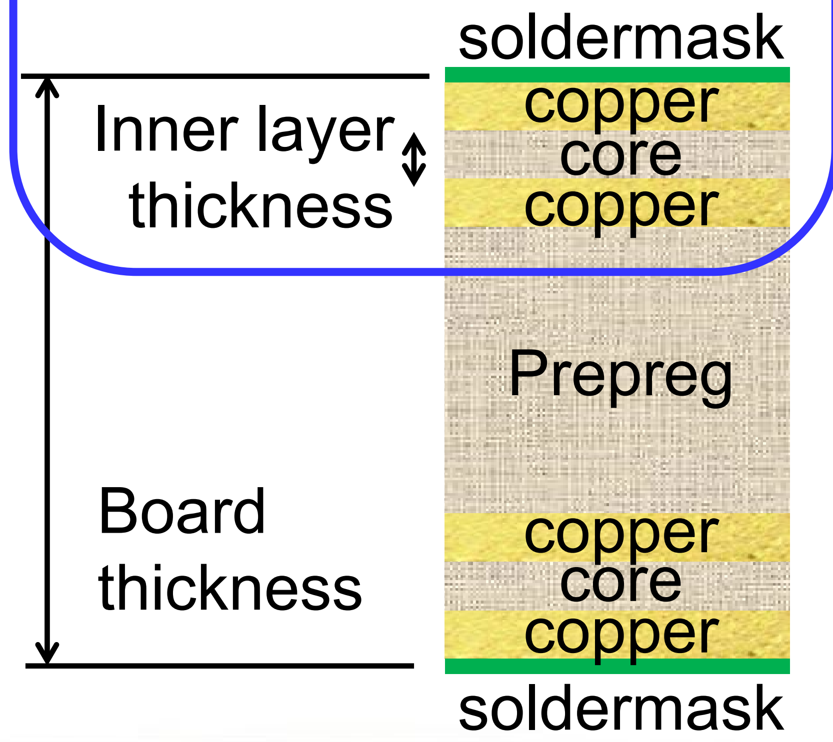


Ext. Vertical



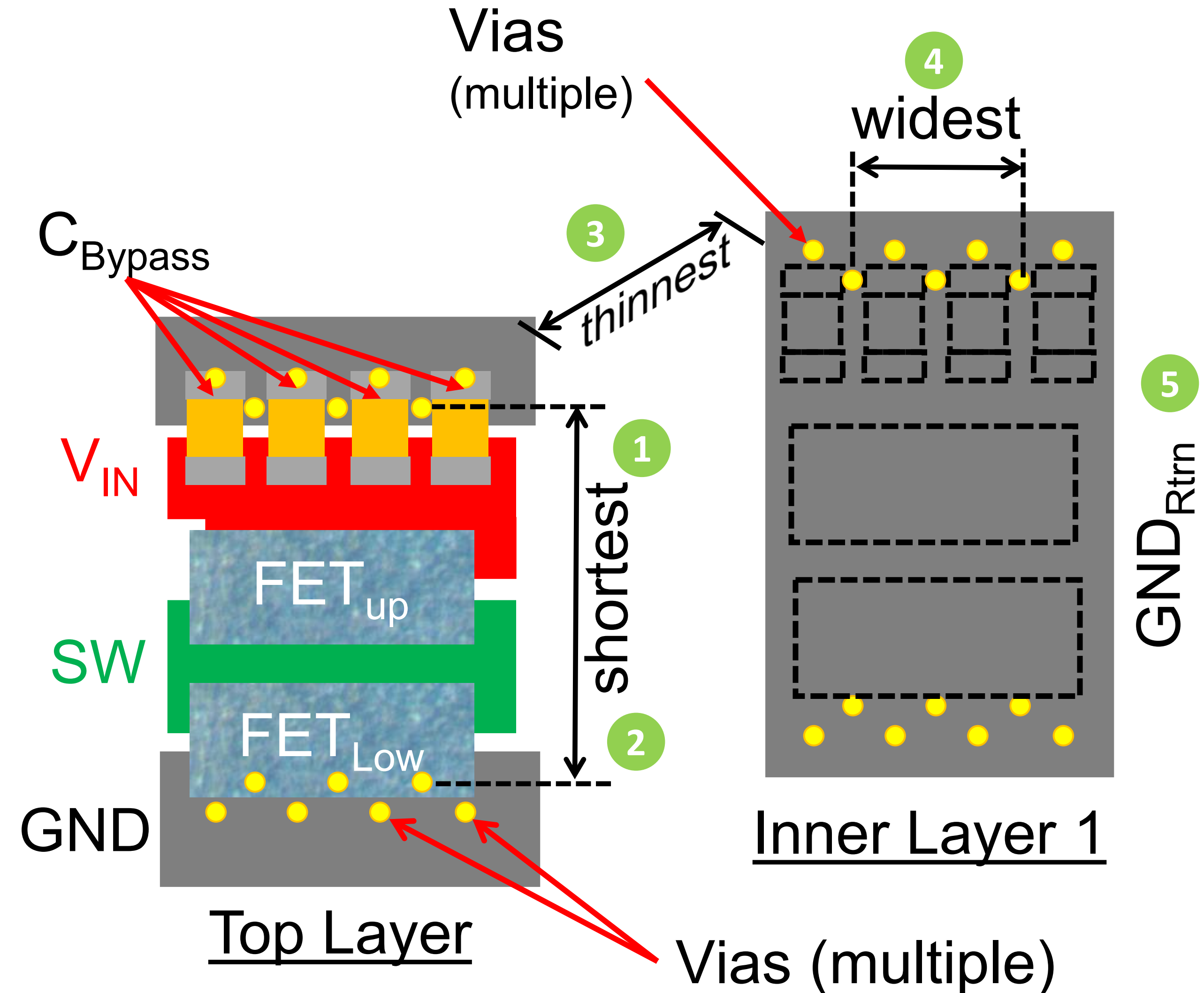
Int. Vertical
Best Choice





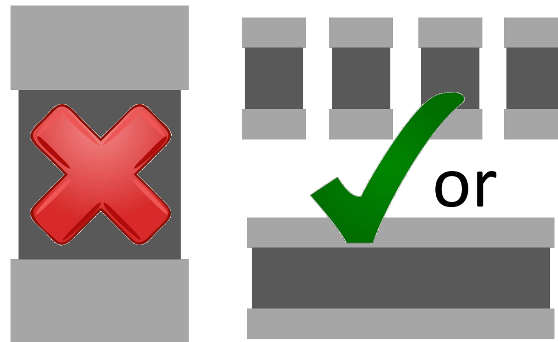
Getting to a Low Inductance Layout

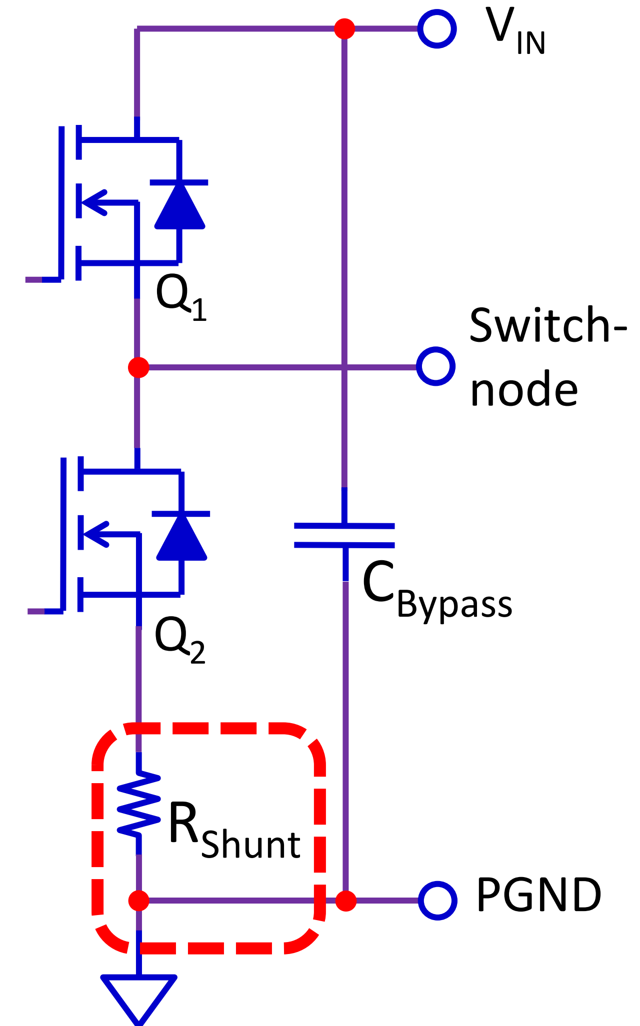
1. Vertically place components as close as possible
2. Place vias as close to the innermost electrical connection
3. Thinnest permissible substrate thickness between outer and first inner layer
4. Spread out via connections at innermost connect
5. GND return does **not** need to carry full current



Considerations for a Source Shunt

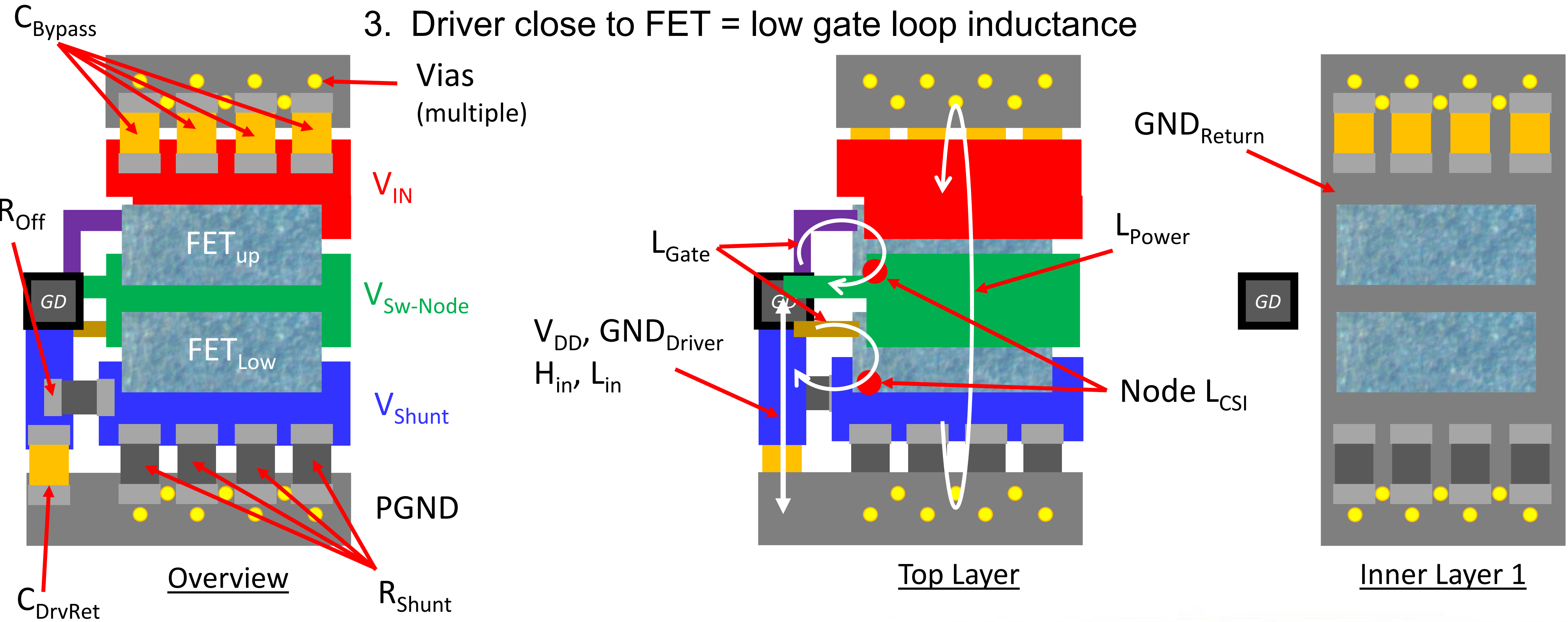
- Treat shunt the same as the decoupling capacitors
- Shunt must be lowest possible inductance





Source Shunt Layout Overview

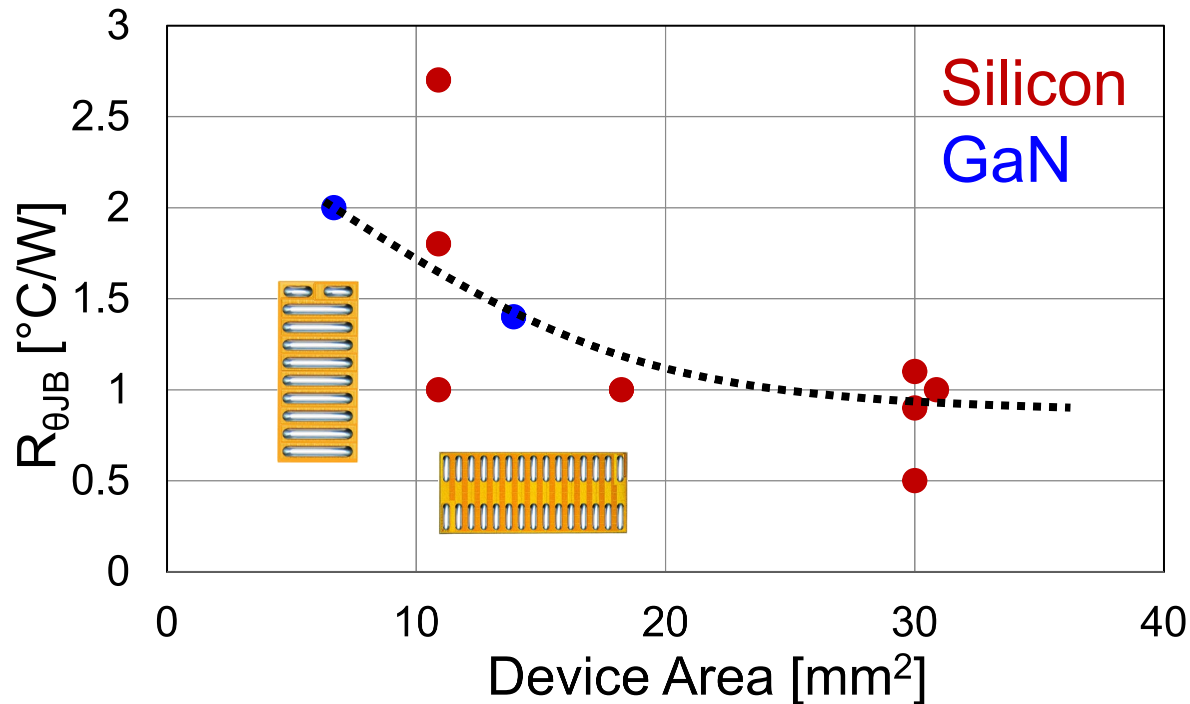
1. Kelvin gate-source return = very low CSI
2. Shunt treated same as decoupling capacitors = Low loop inductance
3. Driver close to FET = low gate loop inductance

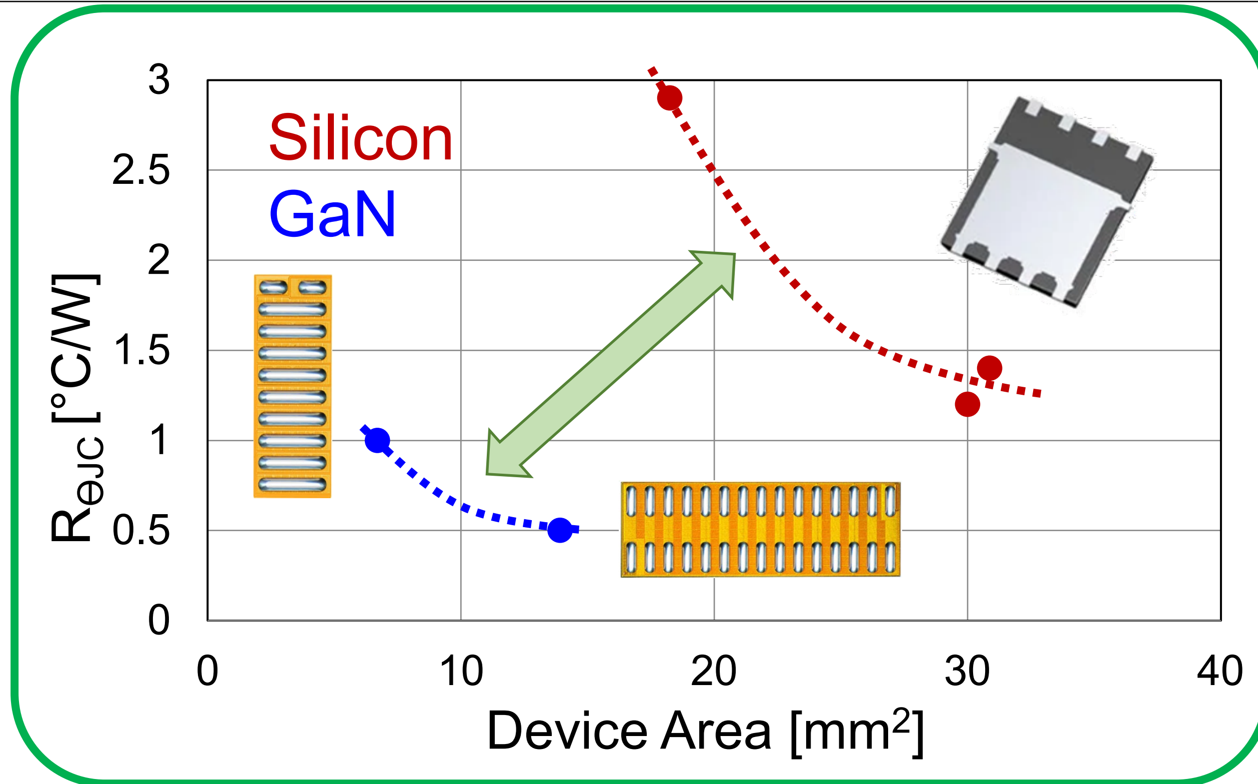


Adding a heatsink to GaN Devices

- GaN device thermal resistance comparisons
- PCB heat-spreading
- Methods to attached a heatsink to GaN FETs
- Online Thermal Calculator overview

Device Thermal Resistance Comparisons

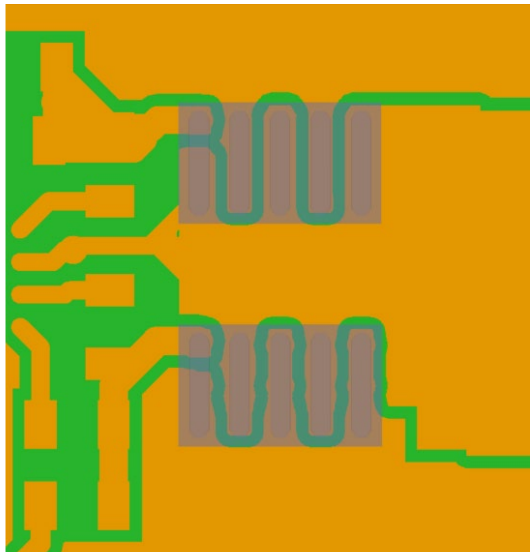




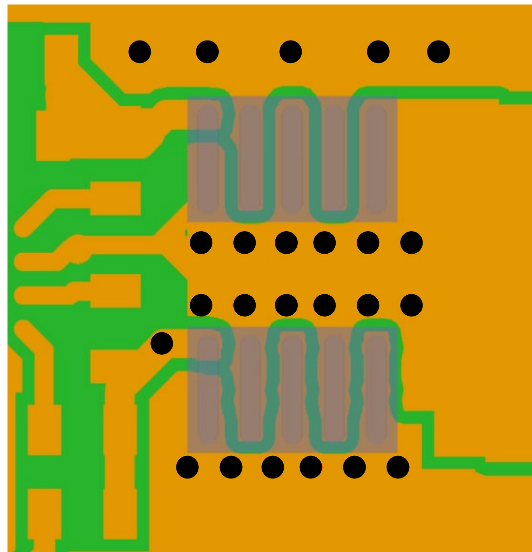
- Small chip scale devices **can** be adequately cooled
- There are simple methods to ensure best thermal practice
- $R_{\theta JC}$ can be used to significant advantage

Using the PCB Copper for Heat-spreading

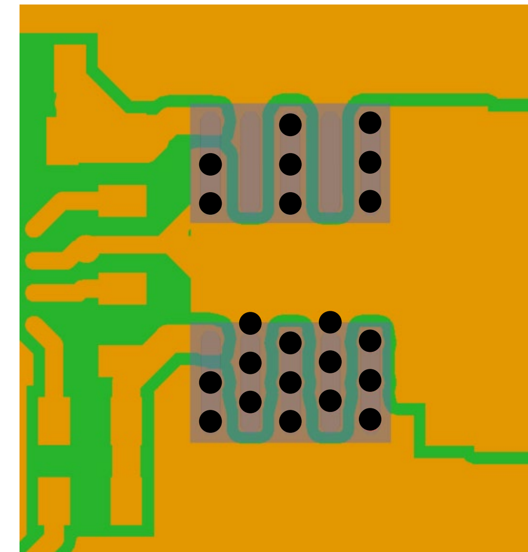
- Copper already in the PCB can conduct heat flux
- Vias can conduct heat flux into inner layers



No Vias



Side Vias



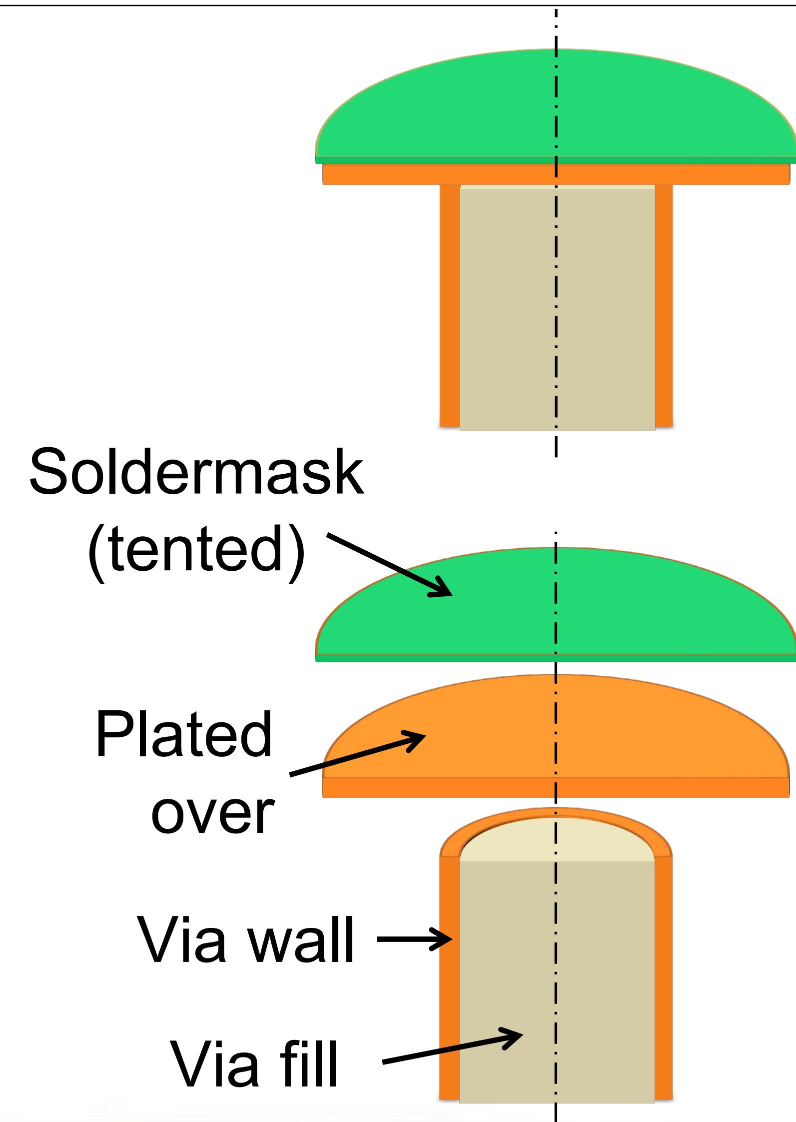
Vias under bump

Spread heat by channeling it into high thermal conductivity layers

Via Construction

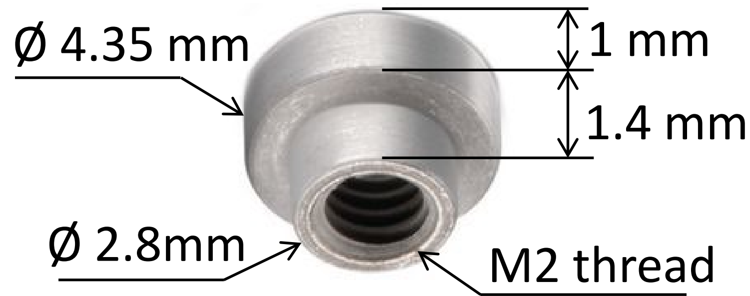
<u>Via-In-Pad-Plated-Over (VIPPO – IPC4761 type VII)</u>

- Wall thickness = 0.78 mil per IPC standard class 2
- Hole diameter (typical) = 7.8 mil
- Annular ring = 13.8 mil diameter min.
- Plated over
- Non-conductive filled
- Tented on both sides of the board
- Used for under bump and close to component pads
- Usable up to 2 oz (2.8 mil / 70 µm) copper thickness



Attaching a Heatsink to GaN FETs

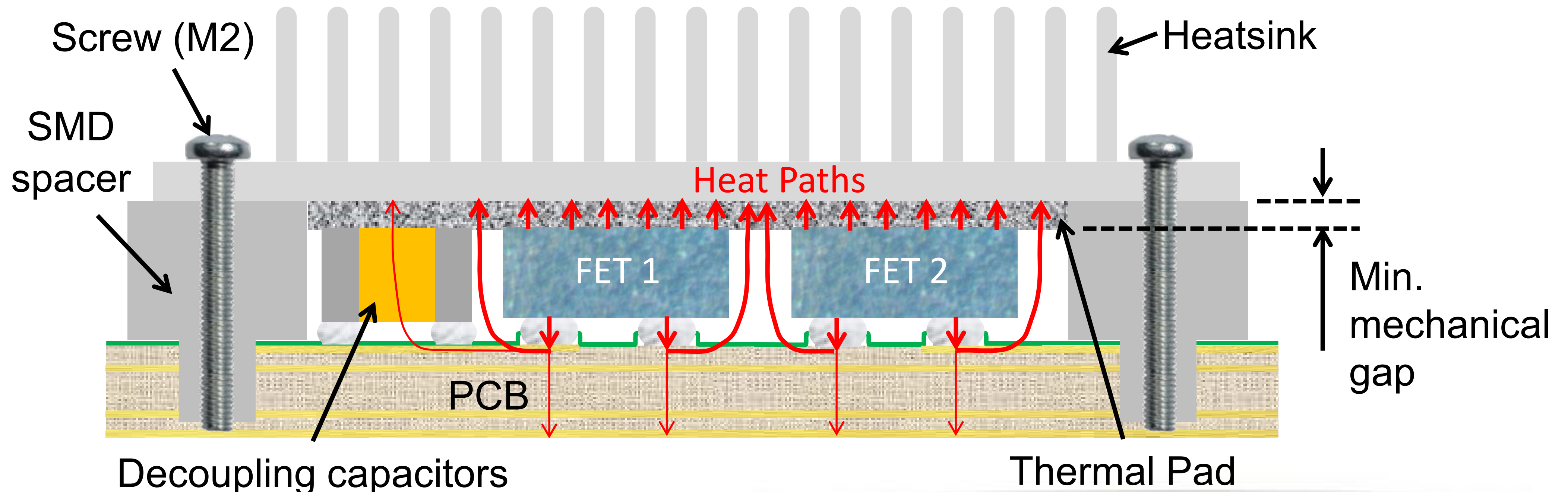
- Simple
- Easy
- Low cost



- Defines space between Gan FET and Heatsink
- Provides means to attach heatsink
- Würth Elektronik P/N 9774010243R

Thermal Approach Cross-section Overview

- All components under heatsink are ≤ height of eGaN FETs
- Thermal pad is mechanically compliant & electrically insulating
  - Example pad: T-Global A1780 (κ =17.8 W/m.K)



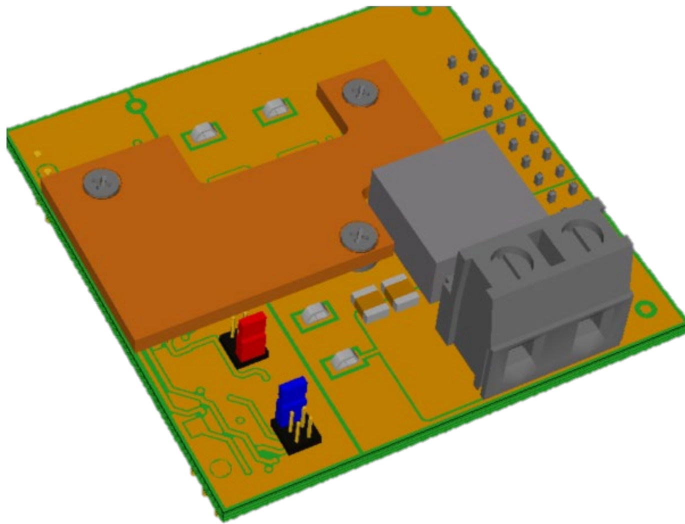
Heat-spreading & Heat-sinking

Heat-spreading

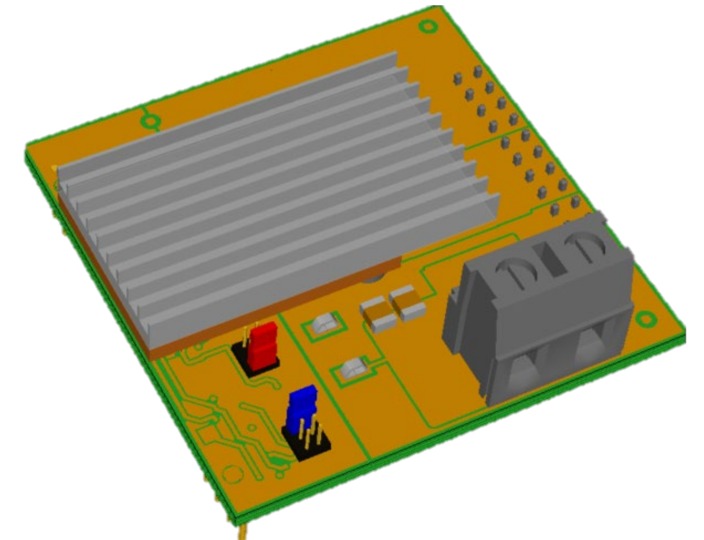
- High thermal conductivity e.g. Copper ($\kappa_{Cu} \approx 400$ W/m·K)
- Effectively increases device thermal area

Heat-sinking

- Aluminum sink added
- Increases surface area for heat flux exchange

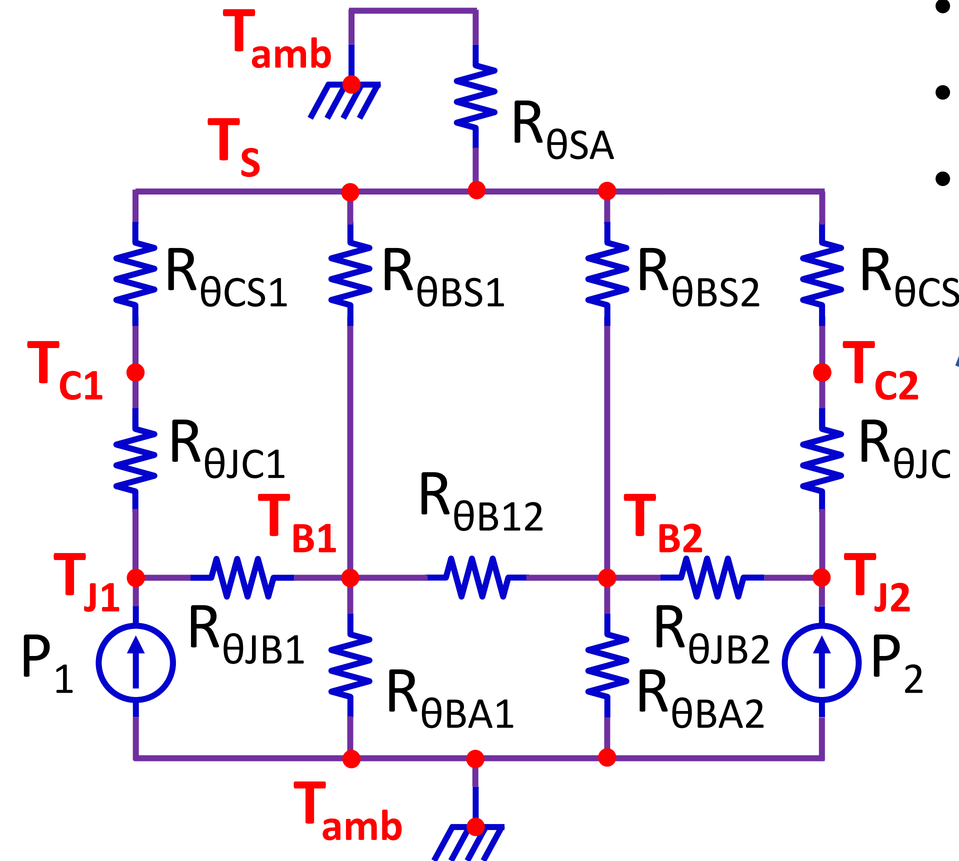


Heat-spreading & sinking can be combined or independent



Heat flux still flows into PCB

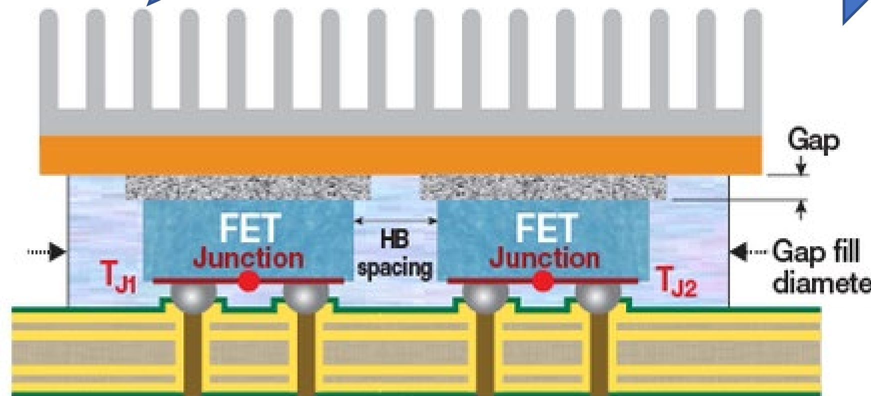
Online Thermal Calculator



Heatsink Thermal Model

EPC's Thermal Calculator:

- Link
- from home page: Design Support, GaN Power Bench
- Choose: FETs, optional vias, optional heat sink, TIM, etc.



Results Summary

Device 1: Junction T (ΔT):

93.0°C (68.0°C)

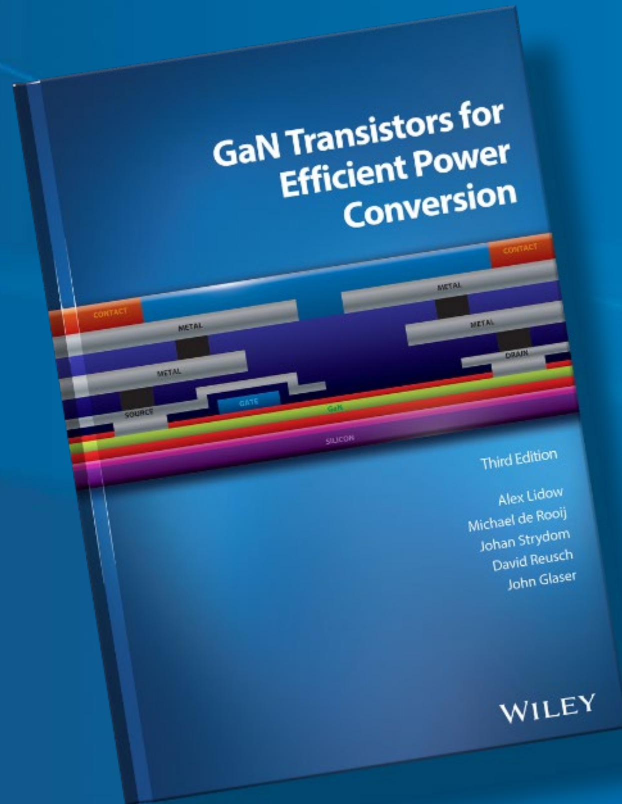
Device 2: Junction T (ΔT):

60.4°C (35.4°C)

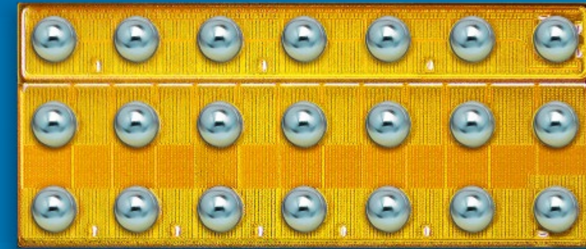
Summer of GaN Webinar Series

- August 3, 2022
  GaN Device Reliability – Proven More Robust than Silicon
- August 17, 2022
  Design Smaller, Lighter, More Efficient Motor Drives with Useful GaN-Based Reference Designs
- September 1, 2022
  Design DC-DC Converters with Higher Efficiency, Smaller Size, and Lower Cost with Useful GaN-Based Reference Designs

How To GaN Video Series

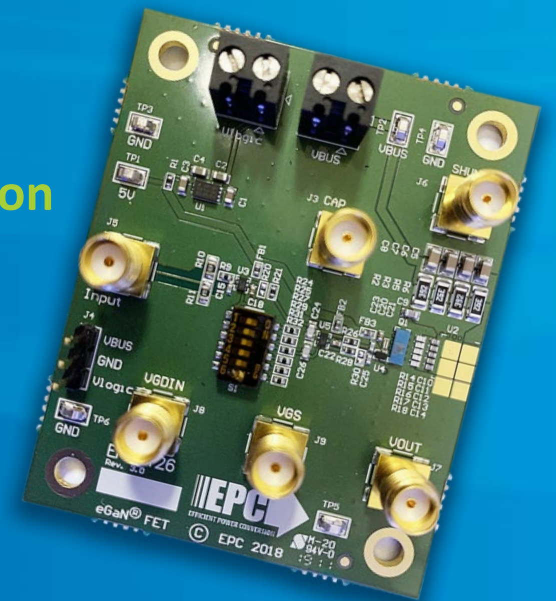


3rd Edition Textbook



eGaN® FETs and ICs

Evaluation Kits



epc-co.com